APPLICATION NOTE

Improved Picture Quality Module MK9

AN97071

Philips
Semiconductors

PHILIPS

Improved Picture Quality Module MK9

Application Note AN97071

Abstract

The Improved Picture Quality (IPQ) module MK9 is an application PC-board designed to evaluate the SAA 4977 or SAA 4974 and demonstrate their features.

The SAA 4977 and the SAA 4974 are video processing ICs providing video enhancing features, memory controlling and an embedded 80C51 µC core. Both are intended to be applied for 50 Hz to 100 Hz (or 60 Hz to 120 Hz) scan conversion using a 2M9 field memory. The SAA 4977 additionally has a built-in analog input interface.

APPLICATION NOTE

Improved Picture Quality Module MK9

AN97071

Author:

Heinrich Waterholter
Systems Laboratory Hamburg,
Germany

Keywords

IPQ
SAA4977
SAA4974
SAA4991
SAA4955
Multi chip module

Date: Sept. 29, 1997

Improved Picture Quality Module MK9

Application Note AN97071

Summary

The SAA 4977 and SAA 4974 are video processing ICs providing video enhancing features, memory controlling and an embedded 80C51 µC core. Additionally the SAA 4977 has a built-in analog input interface. Both are intended to be applied for 50 Hz to 100 Hz (or 60 Hz to 120 Hz) scan conversion using a 2M9 field memory.

This application note gives an overview of the functions of the SAA 4977 and SAA 4974 and describes an application board designed to demonstrate its feature and evaluate the concept. Several grades of IC assembly permit to set up a low, medium and high-end concept of picture improvement. As many functions and features depend on the grade of assembly and the program code implemented on the SAA 4977/74, the relevant software user guide is also necessary for operating the board.

CONTENTS

List of Figures

1. Introduction

The MK9 module is a 100 Hz scan converter based on the video processing IC SAA 4977 or SAA 4974. These ICs make possible a much simpler and cost-effective solution in designing a scan rate converter, compared to previous modules like MK7 or MK6.

With A/D and D/A converters on chip the SAA 4977 needs only one field memory and a display PLL to generate 100 Hz display in an economical A-A-B-B mode. The SAA 4974 does not contain the A/D conversion and analog input interface and is therefore meant to be used with digital input sources.

This application note describes the hardware functions of the SAA 4977 and SAA 4974 and the application environment needed to realize 100 Hz scan conversion as well as extra functions. The internal software of the SAA 4977/74 defines the functions that are available to the user, so to actually run the module and invoke all features the user manual for the implemented software is also necessary. This manual is available as a separate document.[1]

The module MK9 is designed to be assembled with only one field memory besides the SAA 4977 for a low-cost solution, or with two field memories and the SAA 4991 for improved quality scan conversion and extra features.

2. Features of the MK9 IPQ module

The SAA 4977 and SAA 4974 have the following features and functions built-in and therefore simplify the design of a scan rate converter drastically:

Table 1: Features of the SAA 4977 / SAA 4974

Feature	SAA 4977	SAA 4974
Internal prefilter	•	
Clamping	•	
Analog AGC	•	
Triple YUV 8-bit A/D converter	•	
4 : 1 : 1 I/O interfaces	•	
Line locked acquisition PLL	•	
Horizontal compression	•	
Digital color transient improvement (DCTI)	•	•
Luminance peaking	•	•
Triple 10-bit D/A converter	•	•
Memory controller	•	•
Microprocessor with embedded ROM	•	•
I^2C Bus interface	•	•
SNERT interface	•	•

Other features depend on the IC assembly of the board. The following table gives an overview of the available features if the SAA 4977/74 works together with just one field memory of SAA 4955/56 type or an SAA 4991 plus two field memories.

1. Lahann, Nils: I^2C-bus register specification for BESIC, Philips Semiconductors User Manual UM9701

Table 2: Additional features depending on IC assembly

Feature	1 field memory SAA 4955	1 field memory SAA 4956	SAA 4991 + 2 field memories SAA 4955
Scan conversion in A-A-B-B mode (field repetition)	•	•	•
Still picture	•	•	•
Advanced still picture (A-A*-A-A*)			•
Progressive scan			•
Frame repetition mode for movie sources			•
Noise reduction		•	•
Variable vertical zoom			•
Motion vector compensated line flicker reduction			•
Motion vector compensated field rate upconversion			•
Motion vector compensated film processing (conversion from 25 to 50 movement phases)			•

3. Pin list of SAA 4977 and SAA 4974

Table 3: Pin list of SAA 4977 and SAA 4974

Pin	SAA 4977	SAA 4974	Description
1	SDA	SDA	I^2C bus serial port data (PORT1.7)
2	SCL	SCL	I^2C bus serial port clock (PORT1.6)
3	P1.5	P1.5	PORT1 data I/O signal 5
4	P1.4	P1.4	PORT1 data I/O signal 4
5	P1.3	P1.3	PORT1 data I/O signal 3
6	P1.2	P1.2	PORT1 data I/O signal 2
7	P1.1	P1.1	PORT1 data I/O signal 1
8	V_{DDD5}	V_{DDD1}	digital supply (+ 3.3 V)
9	µP_RST	µP_RST	microprocessor reset input (RESET = HIGH)
10	SNRST	SNRST	SNERT restart (PORT1.0)
11	V_{DDD4}	V_{DDD2}	digital supply (+3.3 V)
12	SNDA	SNDA	SNERT data
13	SNCL	SNCL	SNERT clock
14	V_{SSD3}	V_{SSD1}	digital ground
15	TMS	TMS	test mode select
16	V_{SSD1}	V_{SSD1}	digital ground
17	sel_clk	n.c.	select acquisition clock input LOW: external clock; HIGH: internal PLL
18	V_{DDD1}	V_{DDIO1}	digital supply (+5 V)
19	V_{DDD0}	n.c.	digital supply
20	VACQ	VACQ	vertical synchronization input, acquisition part
21	V_{SSA1}	V_{SSIO1}	analog ground
22	HA	HA	analog/digital horizontal reference input

Table 3: Pin list of SAA 4977 and SAA 4974 (continued)

Pin	SAA 4977	SAA 4974	Description
23	V_{DDA1}	n.c.	analog supply
24	RSTW	RSTW	reset write signal output, memory 1
25	V_{DDA2}	n.c.	analog supply (+5 V)
26	Y_in	n.c.	Y analog input
27	V_{SSA2}	n.c.	analog ground
28	U_in	n.c.	U analog input
29	V_{DDA3}	n.c.	analog supply (+5 V)
30	V_in	anatest	V analog input (SAA4974: analog test input)
31	V_{SSA3}	n.c.	analog ground
32	WE	WE	write enable signal output, memory 1
33	LLA_EXT	LLA	acquisition clock input
34	UVod4	n.c.	V digital output bit 0
35	UVod5	n.c.	V digital output bit 1
36	UVod6	n.c.	U digital output bit 0
37	UVod7	n.c.	U digital output bit 1
38	Yod0	n.c.	Y digital output bit 0 (LSB)
39	Yod1	n.c.	Y digital output bit 1
40	Yod2	n.c.	Y digital output bit 2
41	Yod3	n.c.	Y digital output bit 3
42	Yod4	n.c.	Y digital output bit 4
43	Yod5	n.c.	Y digital output bit 5
44	Yod6	n.c.	Y digital output bit 6
45	Yod7	n.c.	Y digital output bit 7 (MSB)
46	V_{DDD2}	V_{DDIO2}	digital supply (+5 V)
47	SWC	SWC	serial write clock output
48	V_{SSD2}	V_{SSIO2}	digital ground
49	TRSTN	TRSTN	test reset, LOW active
50	V_{SSD4}	V_{SSD3}	digital ground
51	Yid7	Yid7	Y digital input bit 7 (MSB)
52	Yid6	Yid6	Y digital input bit 6
53	Yid5	Yid5	Y digital input bit 5
54	Yid4	Yid4	Y digital input bit 4
55	Yid3	Yid3	Y digital input bit 3
56	Yid2	Yid2	Y digital input bit 2
57	Yid1	Yid1	Y digital input bit 1
58	Yid0	Yid0	Y digital input bit 0
59	UVid7	UVid7	U input bit 1
60	UVid6	UVid6	U input bit 0
61	UVid5	UVid5	V input bit 1
62	UVid4	UVid4	V input bit 0

Table 3: Pin list of SAA 4977 and SAA 4974 (continued)

Pin	SAA 4977	SAA 4974	Description
63	RE	RE	read enable signal output, memory 1
64	IE2	IE2	input enable signal output, memory 2
65	V_{SSIO}	V_{SSIO3}	I/O ground
66	BLND	BLND	horizontal blanking signal output, display part
67	V_{DDIO}	V_{DDIO3}	I/O supply (+5 V)
68	HRD	HRD	horizontal reference signal output, deflection part
69	V_{DDD3}	V_{DDD3}	digital supply (+3.3 V)
70	LLD	LLD	display clock input
71	HDFL	HDFL	horizontal synchronization signal output, deflection part
72	VDFL	VDFL	vertical synchronization signal output, deflection part
73	V_{SSA4}	V_{SSA4}	analog ground
74	V_out	V_out	V analog output
75	V_{DDA4}	V_{DDA4}	analog supply (+3.3 V)
76	U_out	U_out	U analog output
77	anaref	anaref	analog reference input
78	V_{SSA5}	V_{SSA5}	analog ground
79	Y_out	Y_out	Y analog output
80	V_{DDA5}	V_{DDA5}	analog supply (+3.3 V)

4. Functional description of the SAA 4977

The board can be equipped with either the SAA 4977 or the pin-compatible SAA 4974. The latter one has a reduced number of features, as it lacks the analog input interface. In the following therefore the functions of the SAA 4977 will be described first, and in the next chapter the differences of the SAA 4974 will be pointed out.

The SAA 4977 provides the interfaces for digital video processing in an analog environment, it generates the control signals to run the field memory, it has on board a microprocessor with embedded ROM, and also offers various processing functions on the video data. For performance reasons the IC consists of two chips (multi-chip module), the first one (acquisition chip) providing mostly analog functions and the second one (display chip) mainly digital functions and controlling. Fig. 1 shows the block diagram of the SAA 4977.

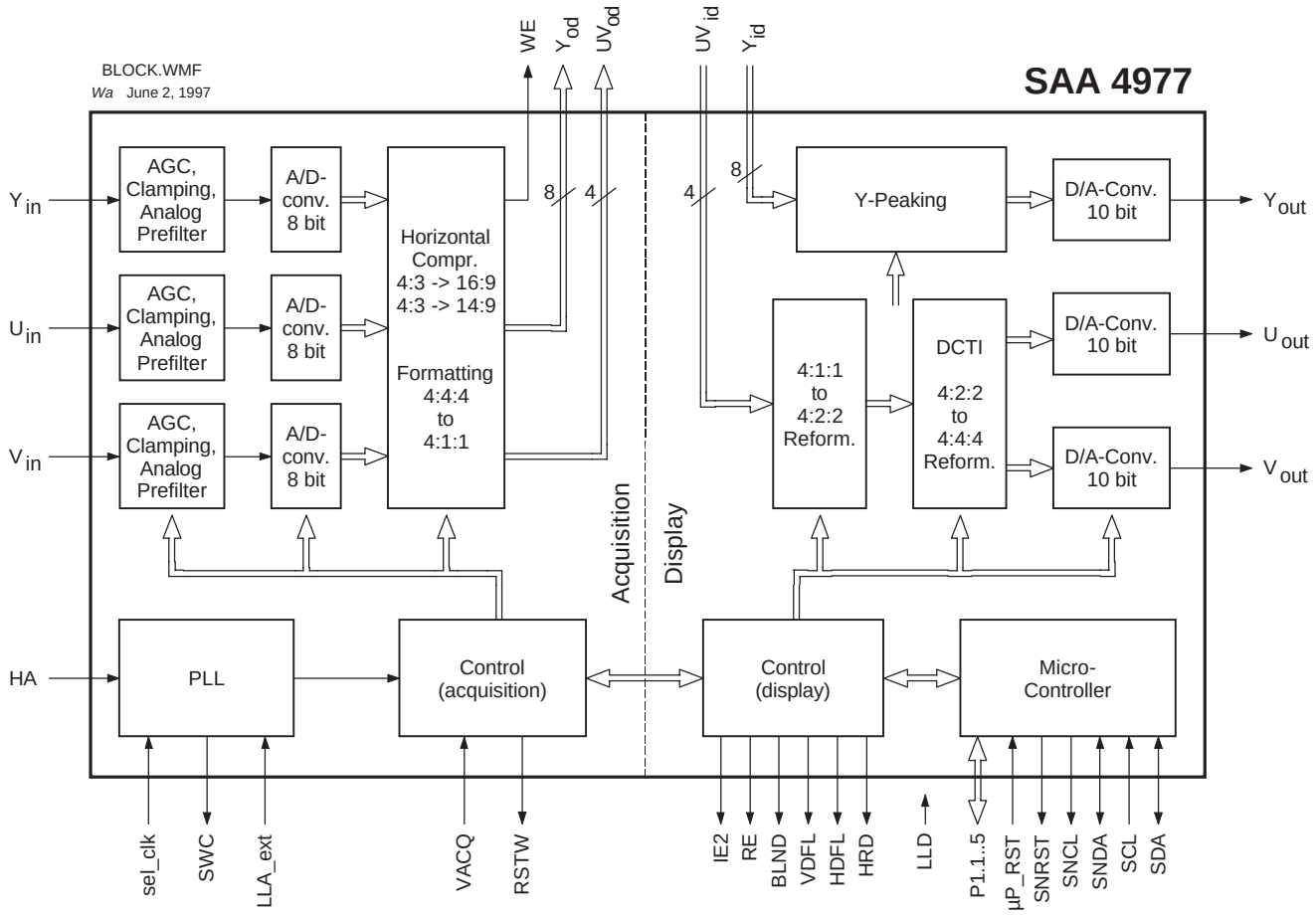


Fig. 1 Block diagram of the SAA 4977

4.1 Analog input processing

At the input of the acquisition chip each of the analog input signals Y, U and V is gain controlled, clamped and low pass filtered, before it is converted to the digital domain by three 8-bit A/D converters.

The gain control unit permits an amplification of -3 dB to +6 dB in steps of 0.4%, a step size hardly visible. Luminance and chrominance gain settings can be controlled separately. The settings are under control of the microcontroller which is therefore needed to set up an automatic gain control loop.

Each input channel has its clamping circuit. For luminance the black level is set to digital level 16, for U and V the colorless level is set to the center level of the A/D converters. The clamping pulse is generated internally.

Before the signals are A/D converted they pass an analog low pass prefilter. The bandwidth of this filter is -3 dB at 6 MHz, a notch is provided at f_{clk} (16 MHz). For the prefilter a bypass can be activated.

Three A/D converters are used to convert Y, U and V into digital data. They are identical, are 8 bit wide and run at 16 MHz data rate.

At the output of the A/D converters an overflow detection is provided. The threshold for this overflow can be selected by software between 216, 224, 232 and 240. The overflow occurrences are summed up in a register the highest 8 bits of which can be read by the microprocessor. In this way an automatic gain control loop can be established.

4.2 Digital processing at $1f_H$ level

Some digital data processing is done at the $1f_H$ level (16 MHz) in the acquisition chip, before data is written to the field memory.

Since all three A/D converters run at 16 MHz, this data format of 4:4:4 needs to be reduced to 4:1:1 to fit into the memory. This conversion is done in two steps. The U and V data are low pass filtered and then down sampled by a factor of two, low pass filtered again and down sampled a second time by a factor of two. Finally the data is formatted into the 4:1:1 format, see fig. 2. In this format the chrominance information is distributed over 4 clock periods, the first data word beginning one clock period after the rising edge of the WE signal.

For displaying a 4:3 sources on a 16:9 screen a horizontal signal compression can be activated. The compression factor in this case is 4/3 = 1.33 (16:9 mode). For a slighter compression mode also 7/6 = 1.16 is selectable (14:9 mode).

When compression is active, a reduced number of pixel data per line is generated. To achieve this at the same clock frequency every 4th (in 16:9 mode) or every 7th (in 14:9 mode) pixel is discarded (memory writing disabled). The remaining ones are derived from an interpolation unit where a variable phase delay filter is used. This filter ensures a high accuracy in interpolation.

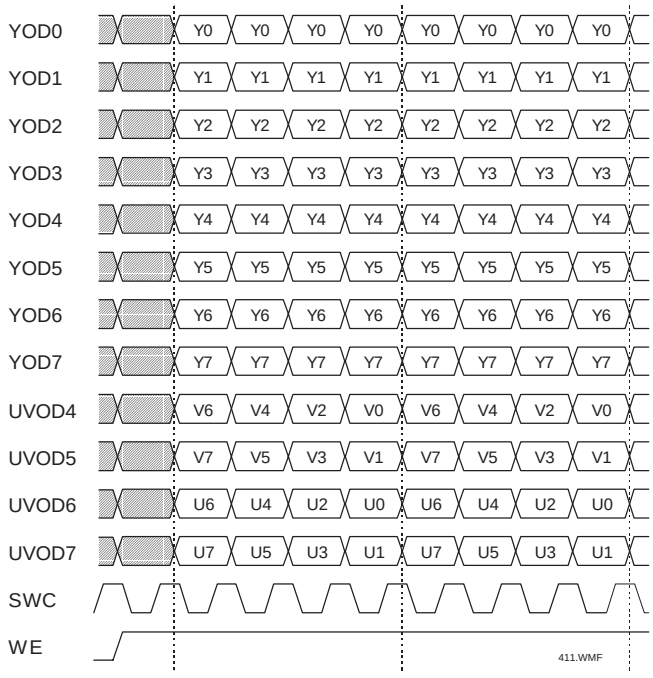


Fig. 2 4:1:1 data format

4.3 Digital processing at $2f_H$ level

From the acquisition chip the digital video data is written to a field memory. Reading is done at twice the clock rate by the display chip of the SAA 4977.

4.3.1 Signal data range

Signal data on the display chip are processed using a 10 bit wide data range. The user can select how this extended range is to be used. In display mode 1 the full 10 bit range is used for the nominal signal. The black level is now at 64 and has the same relative level compared to the 8 bit input signal. In display mode 0 basically a 9 bit range is used for the nominal signal. The black level is at 288 and the white level at 767. This leaves ample room for signal over- and undershoots. These relations are depicted in fig. 3.

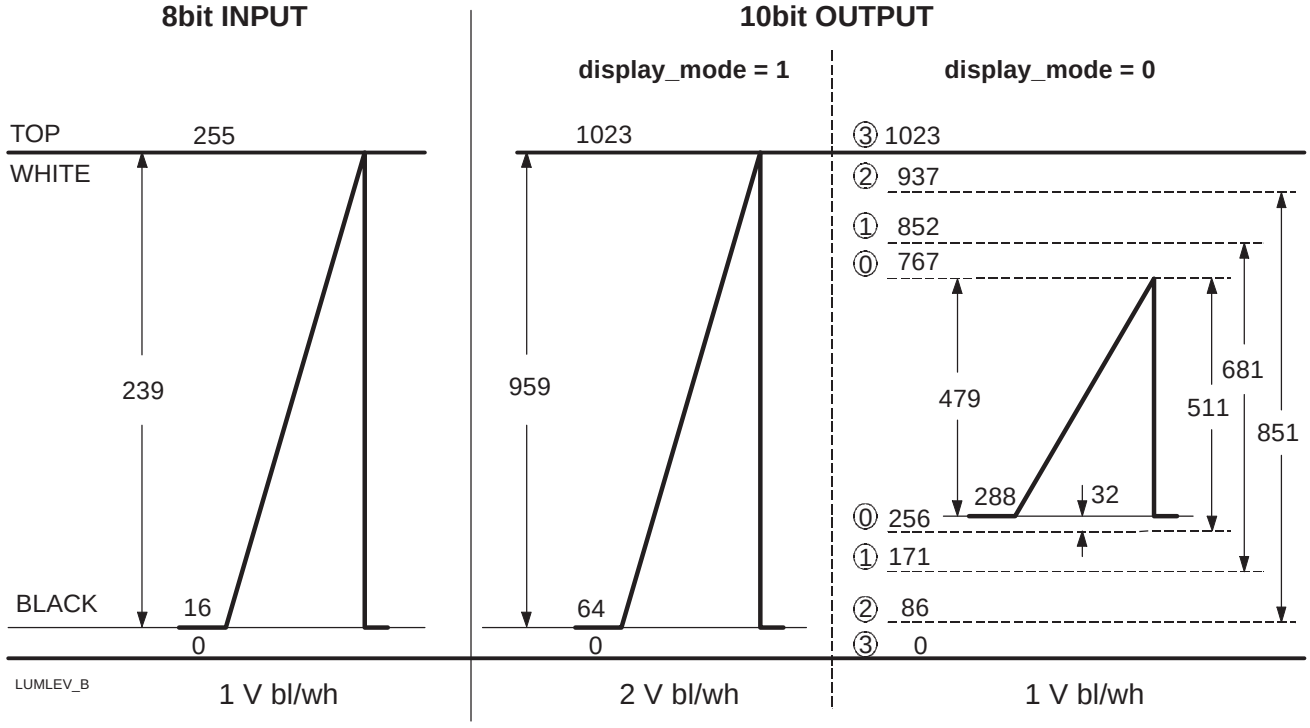


Fig. 3 Display modes

limit_set = 0, 1, 2, 3 :
limiting levels ⓪ ① ② ③

4.3.2 Luminance Peaking

The luminance signal Y is processed by the linear peaking circuit of the display chip in order to boost the higher frequency ranges. A block diagram of the circuit is shown in fig. 4. The circuit uses a combination of band pass filter and high pass filter having their maximum gain at f_c /4 and f_c /2 resp., the output of which is added to the original signal. The influence of each of the filters can be adjusted in four steps. In fig. 5 to 8 the frequency response of the peaking circuit is given for different values of alpha (middle range) and beta (upper range).

The over- and undershoots generated by the peaking circuit can be limited, depending on far they exceed the nominal range of the output signal. The relations are shown in fig. 3, right-hand side. For *limit_set* = 0 the limiting levels 0 are valid and the output range is limited to 511 +256 / -255 = 256...767, thus leaving practically no room

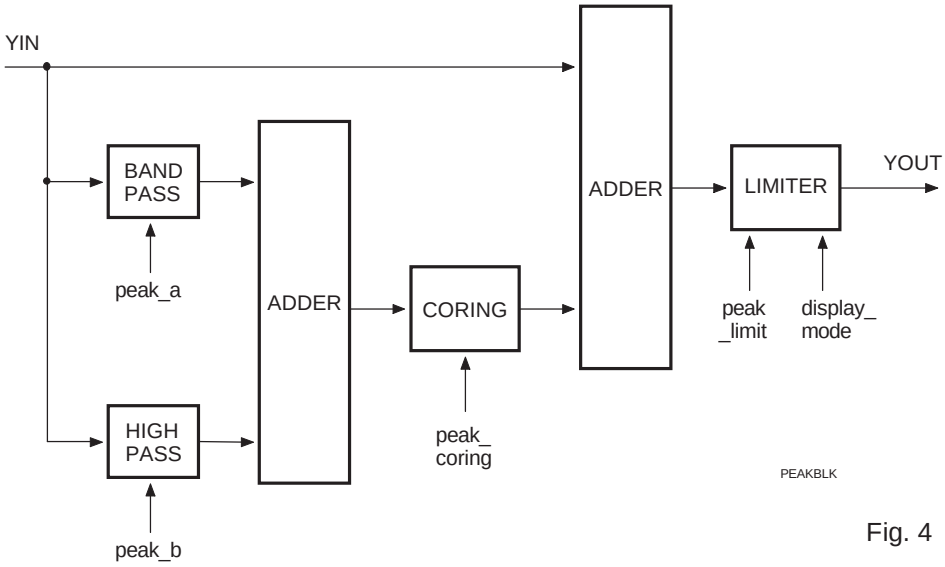


Fig. 4 Peaking block diagram

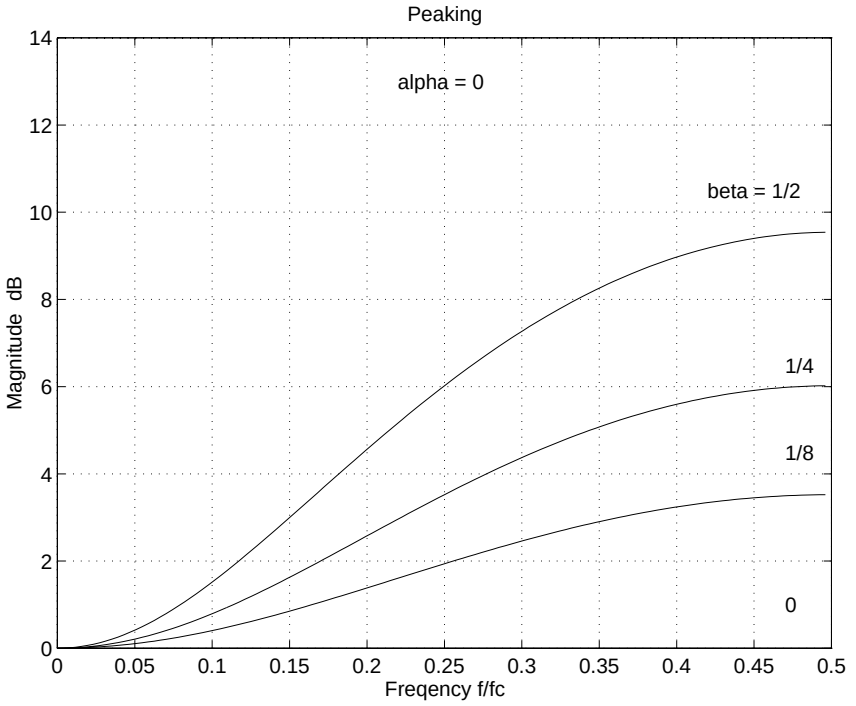


Fig. 5
Frequency response of the peaking filter for alpha = 0

for signal amplitudes exceeding the nominal range. For *limit_set* = 1 and 2 the tolerated range is extended to 171...852 and 86...937 until at *limit_set* = 3 the total 10 bit range of 0...1023 is used.

The peaking filter will boost higher frequency signals regardless of their amplitude. For structured small signals this will lead to unwanted coring. In order to prevent this the coring block is added. It suppresses any gain for low amplitudes, so the original luminance signal is not influenced. Coring levels that can be programmed are 0 (no coring), 4, 8 and 16. The different transfer curves are depicted in fig. 9.

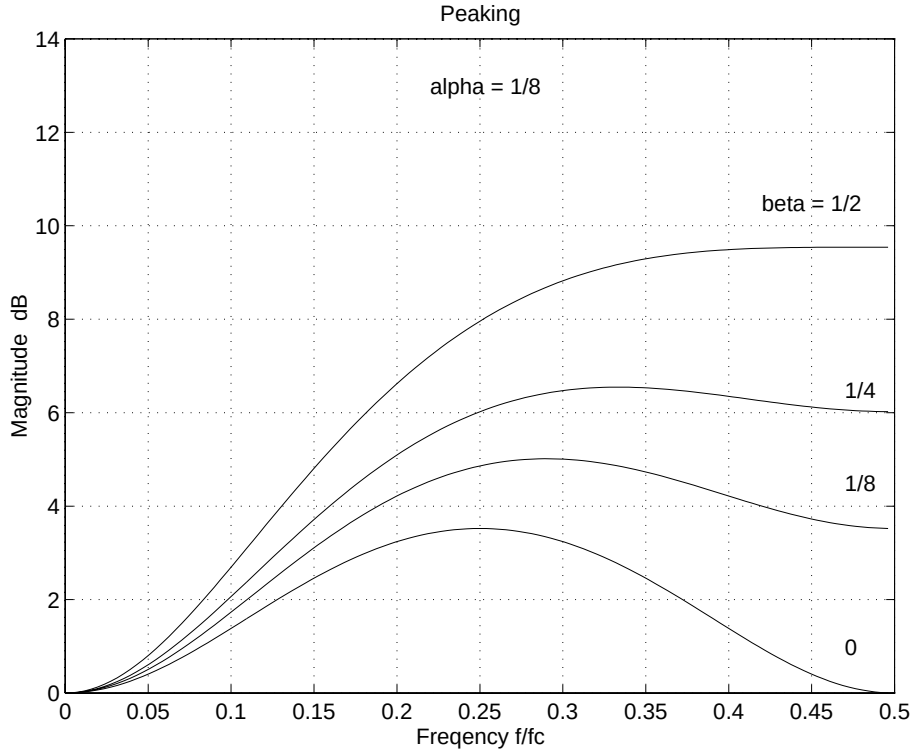


Fig. 6
Frequency response of the peaking filter for alpha = 1/8

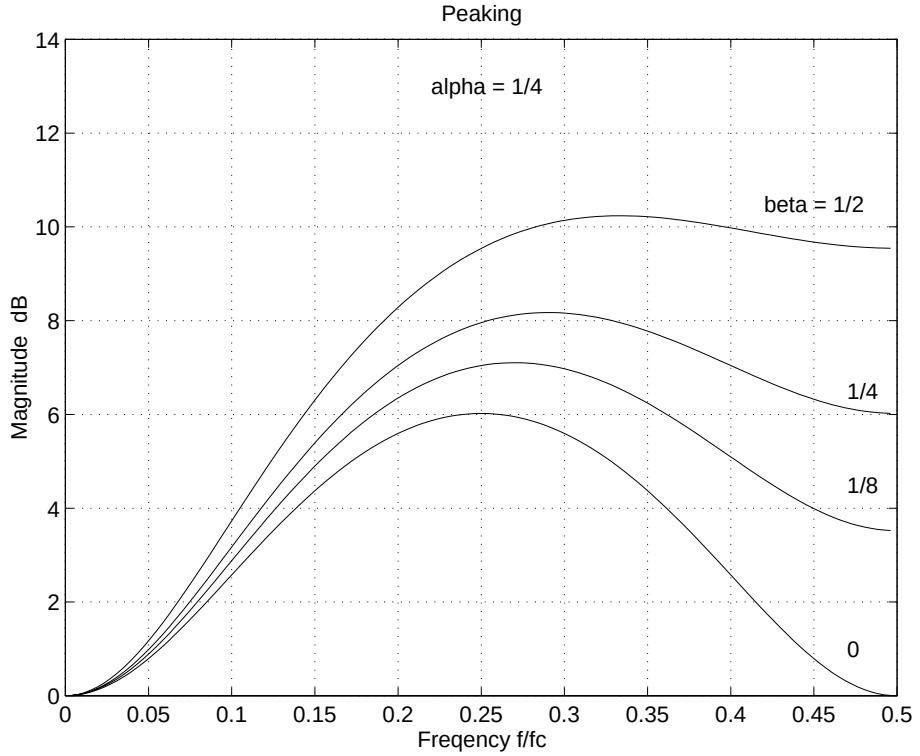


Fig. 7
Frequency response of the peaking filter for alpha = 1/4

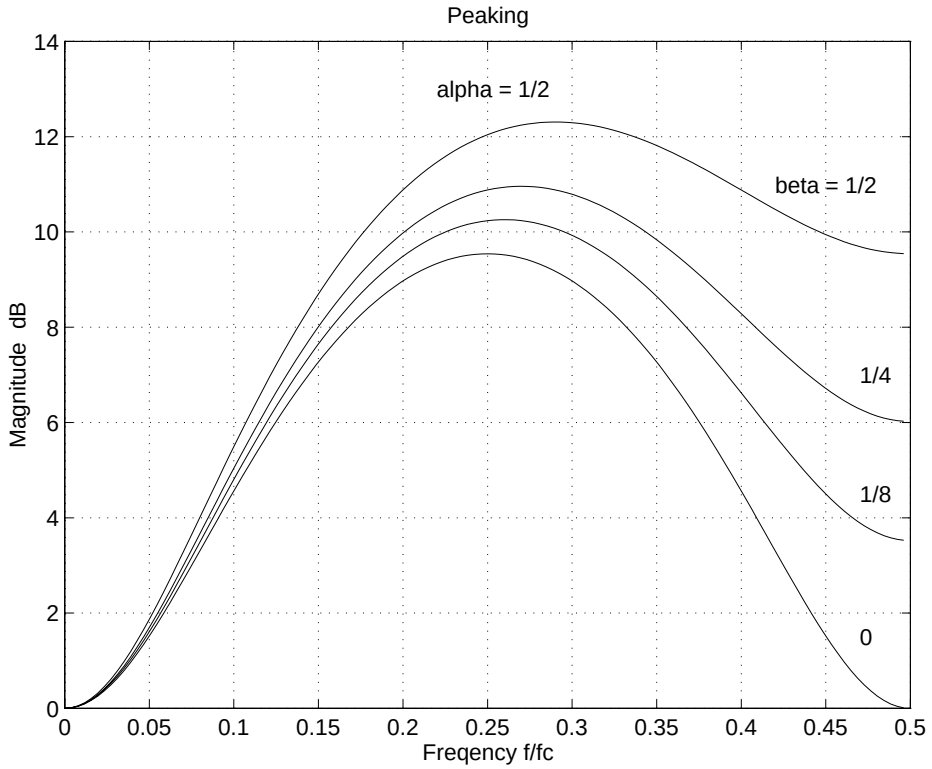
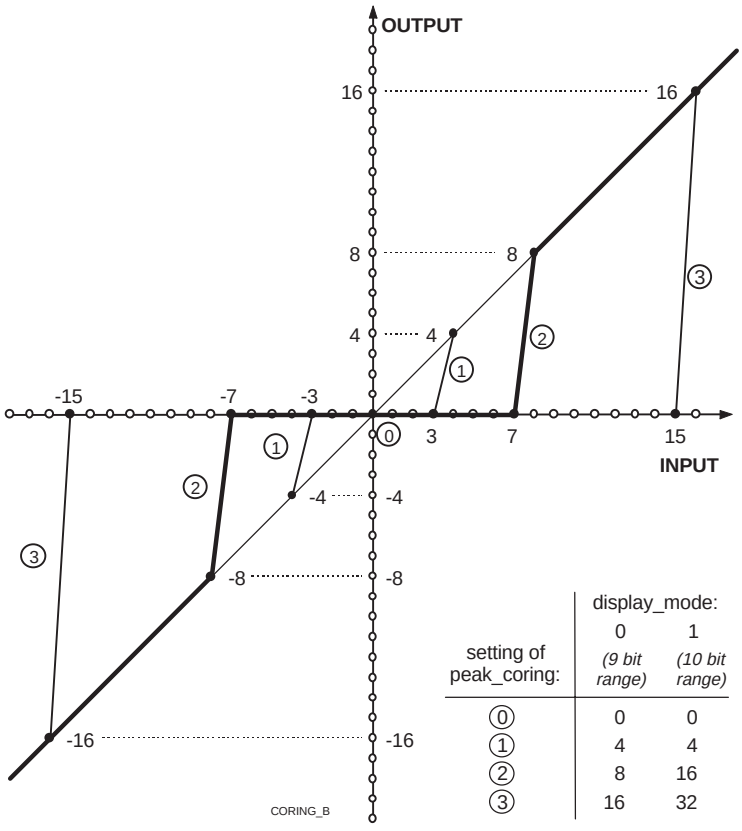


Fig. 8
Frequency response of the peaking filter for alpha = 1/2



setting of peak_coring:	display_mode: 0 *(9 bit range)*	display_mode: 1 *(10 bit range)*
⓪	0	0
①	4	4
②	8	16
③	16	32

Fig. 9 Luminance coring

4.3.3 Digital color transient improvement (DCTI)

U and V data are reformatted from 4:1:1 to 4:2:2 using a linear interpolating filter. Further upsampling to the 4:4:4 format occurs during the DCTI process.

The Digital Color Transient Improvement (DCTI) is intended for U and V signals originating from a 4:1:1 source. Horizontal transients are detected and enhanced without generating overshoots.

The data path delay is varied on the basis of a function of the second derivative of the U and V signal. The effect at an edge is that during the first half the data path delay is higher than nominal and in the second half it is lower than nominal. This will make the edge much steeper. As this interpolation is done with the resolution equal to that of the Y samples a 2:1 interpolation is performed generating a 4 :4 :4 format for the D/A converters.

The DCTI function can be controlled mainly by adjusting the parameters *gain* and *limit*. *Gain* influences the resulting steepness of the output signal, whereas *limit* affects the maximum amount of data path delay. Modifications of these parameters are depicted in the fig. 10 and fig. 11 using a maximum amplitude color transient as input signal. Both *gain* and *limit* must be greater than zero for DCTI to be active.

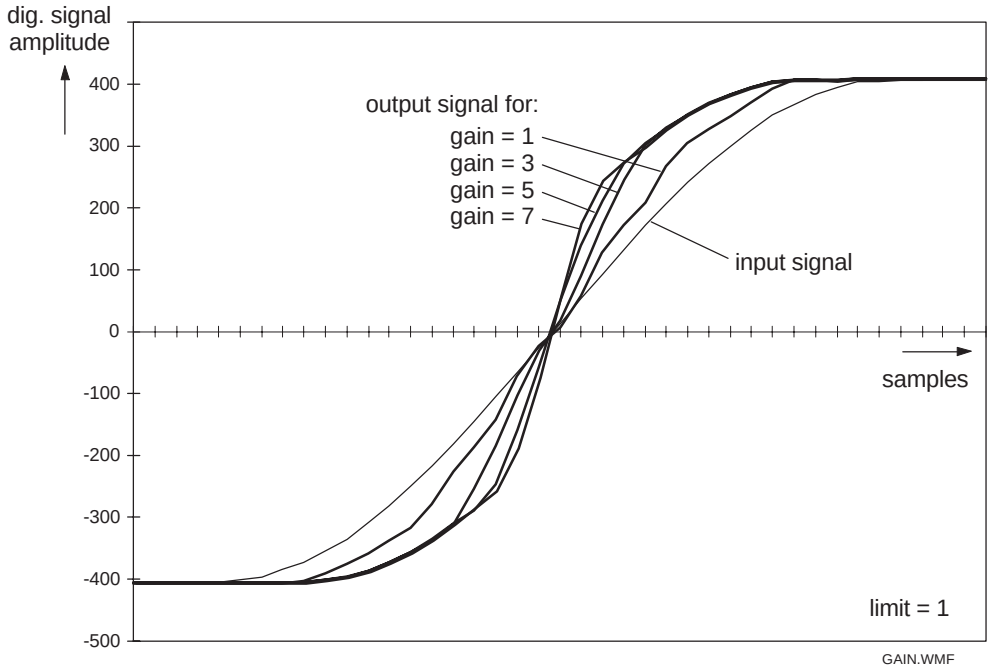


Fig. 10 DCTI with variation of gain for a limit setting of 1

An artifact of this processing becomes apparent when two edges are close together in the video. During the second half of the first edge a delay is chosen that will collect video data from where the second edge is already active. The same is valid for the second edge. The result of this processing on a video pulse, which is looking like a hill, is that of a hill with one or two bumps on it. To prevent this from happening, the positions where the first derivatives in U and V change sign, are marked and used to limit the range of the relative delay. This function is called ‘over-the-hill protection’. It can be turned on and off. Figures 12 and 13 show the effect of the DCTI function with and without ‘over the hill protection’ when applied to a hill-shaped video pulse.

The ‘hill protection‘ function still produces artefacts for signal transitions where the first derivative does not change sign, i. e. two (or more) positive (or negative) steps following each other. Signals of this kind are handled properly if ‘superhill protection‘ is turned on. The behavior of DCTI with active and inactive ‘superhill protection‘ is shown in fig. 14 and 15. Slight overshooting occurs if the output filter is turned on.

The DCTI function can be controlled by the parameter *separate* in regard to whether both signals U and V are processed together or each one separately. In case of *separate* = 0 (off) a steep transition in either signal is suf-

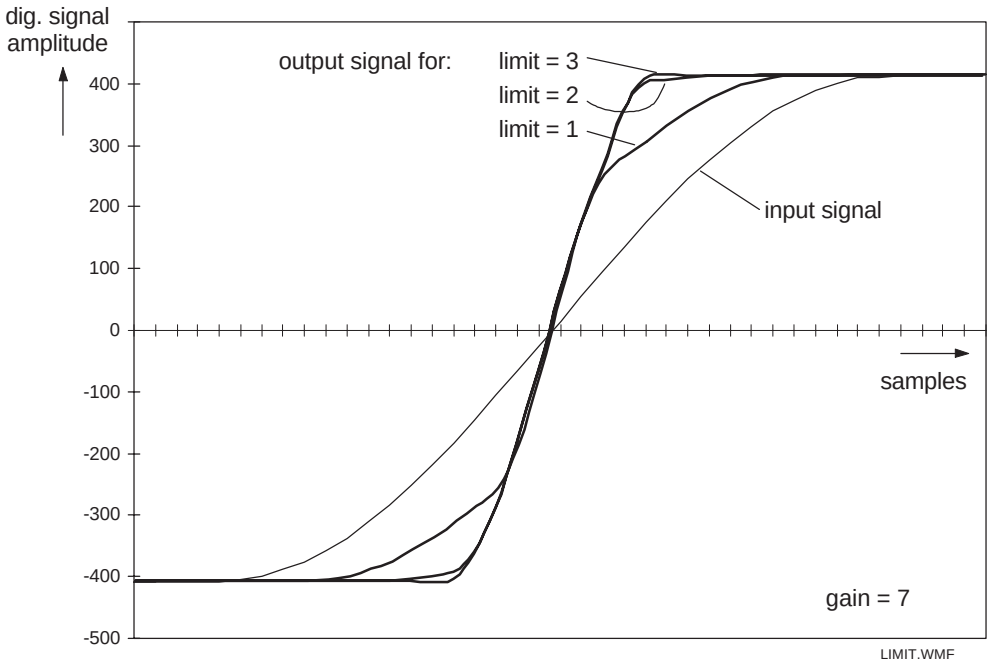


Fig. 11 DCTI with variation of limit for a gain setting of 7

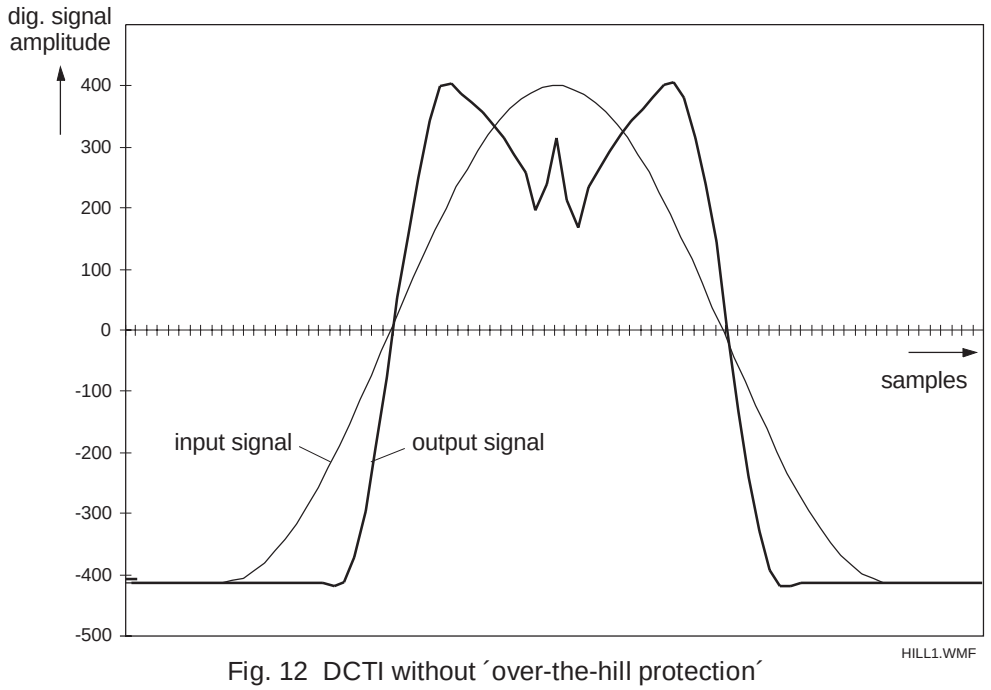


Fig. 12 DCTI without ´over-the-hill protection´

ficient to activate the data path delay variation. This setting is based on the fact that most color transients involve both signals U and V. And if one of the signals stays constant, a data path variation would do no harm.

In case of *separate* = 1 (on) each signal is processed separately. This setting is favorable if the transitions in both signals do not occur at the same time. Common processing then would give false colors which can be annoying. An example for processing such signals is given in fig. 16 and 17.

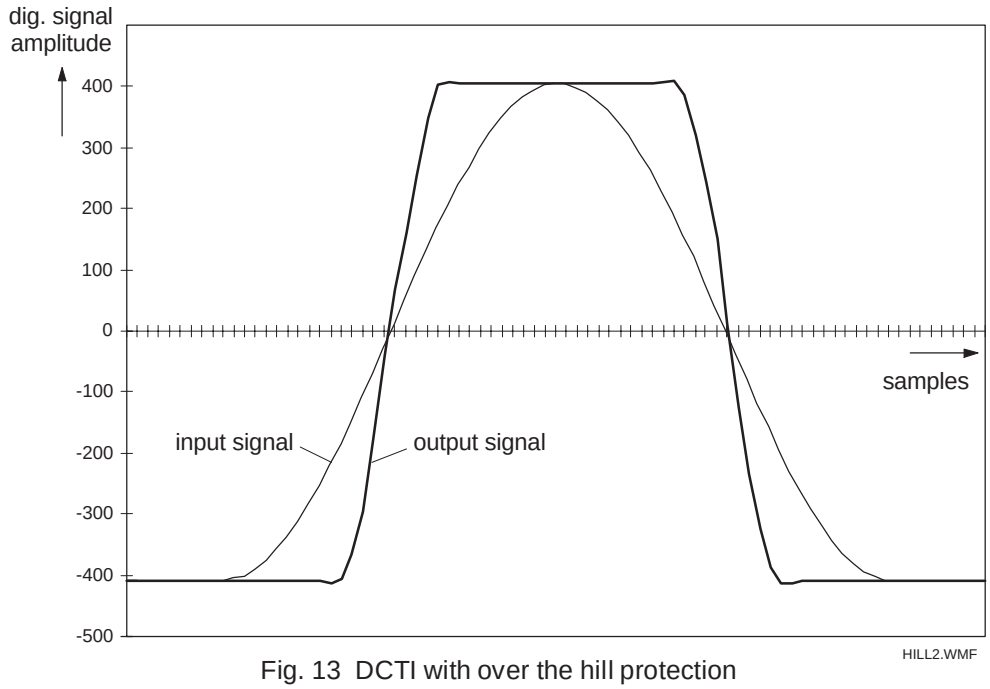


Fig. 13 DCTI with over the hill protection

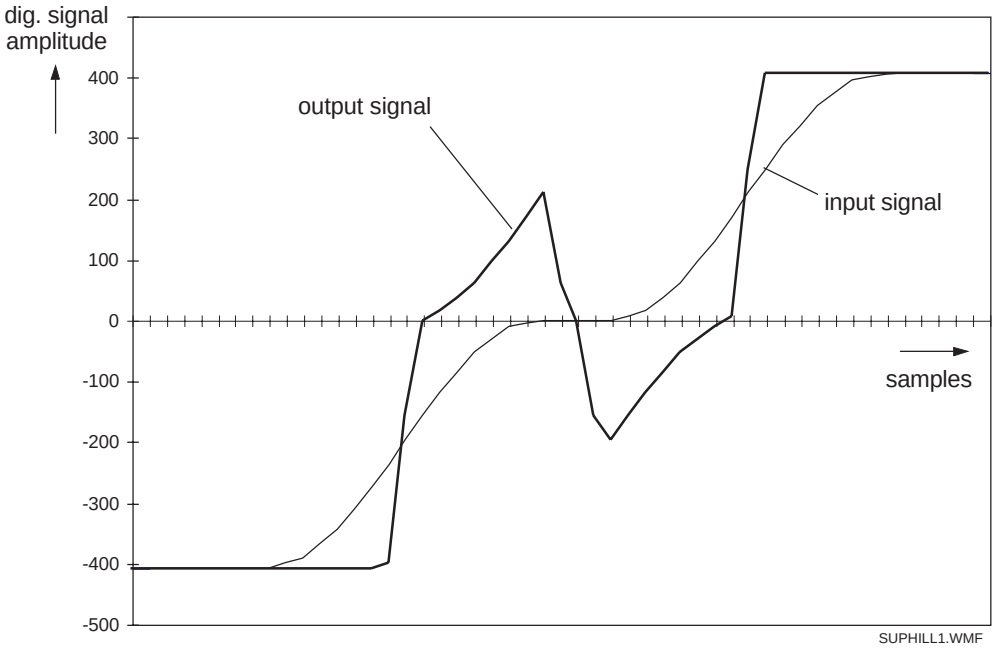


Fig. 14 DCTI with superhill-protection off

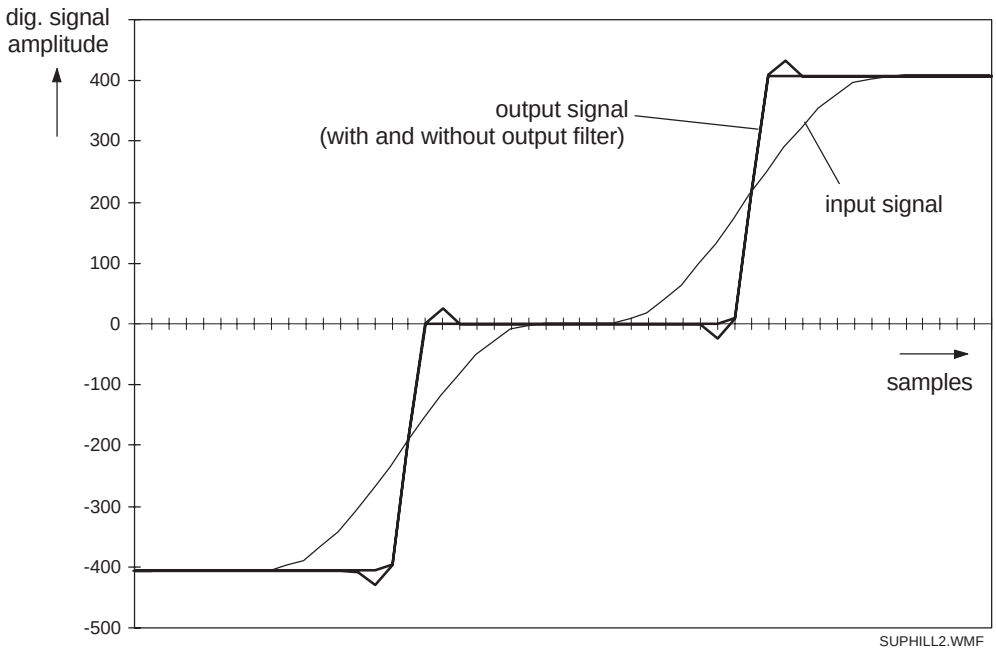


Fig. 15 DCTI with superhill-protection on

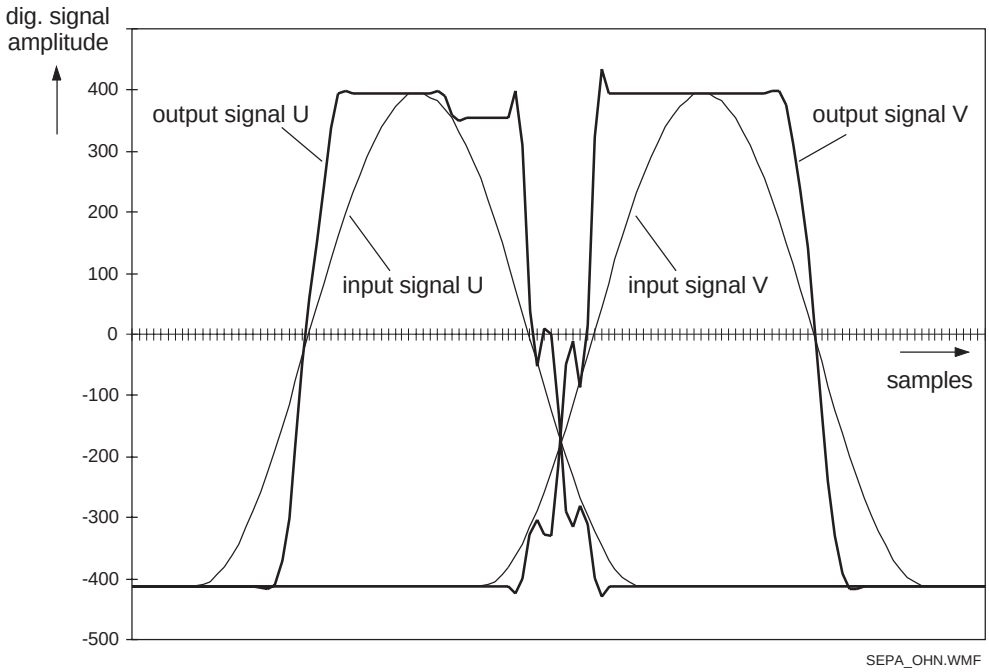


Fig. 16 DCTI with common processing of both signals (*separate* = 0)

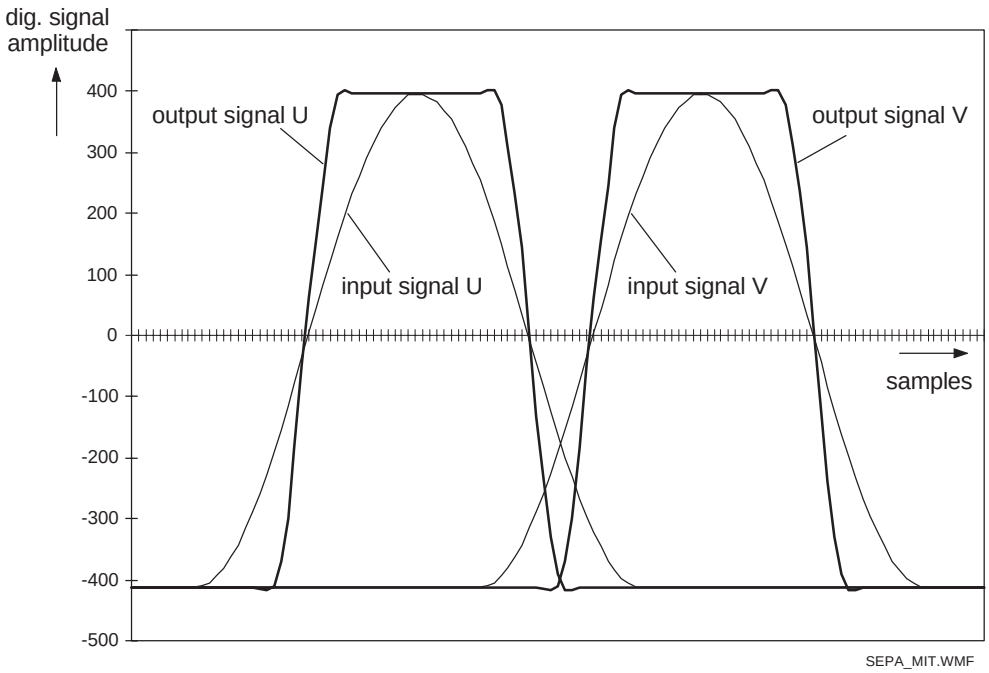


Fig. 17 DCTI with separate processing of both signals (separate = 1)

4.4 Controlling

Both the SAA 4977 and SAA 4974 contain an on-chip microcontroller and a memory control unit that generates the required signals to run the field memories. On the SAA 4977 this control unit is divided into an acquisition and a display part, each on the respective chip. On the SAA 4974 both parts are combined.

Only the SAA 4977 has an acquisition PLL circuit, so it can generate its own acquisition clock or run on an external one. The SAA 4974 only has this external clock mode.

4.4.1 Acquisition PLL

The acquisition PLL is on the acquisition chip of the SAA 4977. The rising edges of the external HA signal (horizontal acquisition pulse or H_{sync}) and the internally generated H_{ref} are compared, and the measured phase difference controls a clock generator. This clock generator runs at 32 MHz with a simple clock divider being used to generate 16 MHz. This ensures a perfect 50% duty cycle for the system clock LLA[2] of the acquisition chip.

A video line of 64 µs contains 1024 clock cycles of 16 MHz. Therefore the clock frequency is divided by 1024 to get the horizontal reference signal H_{ref}.

The acquisition system clock LLA can also be provided externally. This external clock mode is activated by pulling pin SEL_CLK to LOW, the internal PLL is now switched off. A synchronous H_{ref} signal must be provided at pin HA by the external application.

4.4.2 Memory controller

The on-chip memory controller provides the necessary control signals for one- or two-field memory concepts. The write signals for the first memory are derived from the acquisition clock, signals for reading are derived from the display clock. In order to achieve this the memory controller is divided into an acquisition part and a display part. On the SAA 4977 each part is placed on the resp. chip. An asynchronous serial link provides communication between the two parts.

4.4.3 Microprocessor

The SAA 4977 and SAA 4974 contain an embedded 8051 microprocessor core including 256 Byte RAM and 16 kB ROM (µC). The microprocessor is placed on the display chip and runs on a 16 MHz clock, generated by dividing the 32 MHz display clock by a factor of 2.

A parallel port (PORT 1) can be used for application specific signals. While pins P1.0, P1.6 and P1.7 are already used for SNRST and the I^2C bus signals SCL and SDA resp., the port pins P1.1 ... P1.5 are still available for specific purposes.

Internally the microprocessor and the display part of the memory controller are connected by a parallel address and data bus. Via this bus the µC communicates with all parts of the chip. The memory controller serves as a router, distributing all display related write and read controls on the display chip and sending/receiving all acquisition related data via the serial link to/from the acquisition chip.

For communication with external ICs two serial busses can be used, the I^2C bus and the SNERT bus. The I^2C-bus interface is used in a slave receive and transmit mode for general communication with a central master microcontroller. Both standardized baud rates of 100 kBit/s and 400 kBit/s are supported.

The SNERT[3] bus is used for communication with slave ICs that also have this interface. It is a single master bus and uses the µC´s serial interface for transmitting and receiving data. Clock is supplied by pin SNCL while data is written or read through pin SNDA. These pins refer to the pins TxD and RxD of a standard 8051 µC, and the transfer mode is known as mode 0 of the serial interface. Address and data bytes are transmitted alternately. As reset signal the bus uses a third signal line (SNRST) to determine the correct address / data sequence as well as

2. LLA ... *Line Locked Acquisition* (clock)
3. SNERT stands for *Synchronous No-parity Eight bit Reception and Transmission*

to update any readable registers in the devices. In a video environment however the vertical sync pulse is usually taken for this reset purpose, since SNERT transmissions are initiated by this pulse, too.[4]

5. Functional description of the SAA 4974

If digital input signals are available, e. g. from a digital color decoder, the SAA 4974 can be used instead of the SAA 4977. The acquisition chip containing the analog input interface is missing, so the SAA 4974 consists of the display chip alone, which is modified somewhat, so it can run as a stand-alone device. Fig. 18 shows the block diagram.

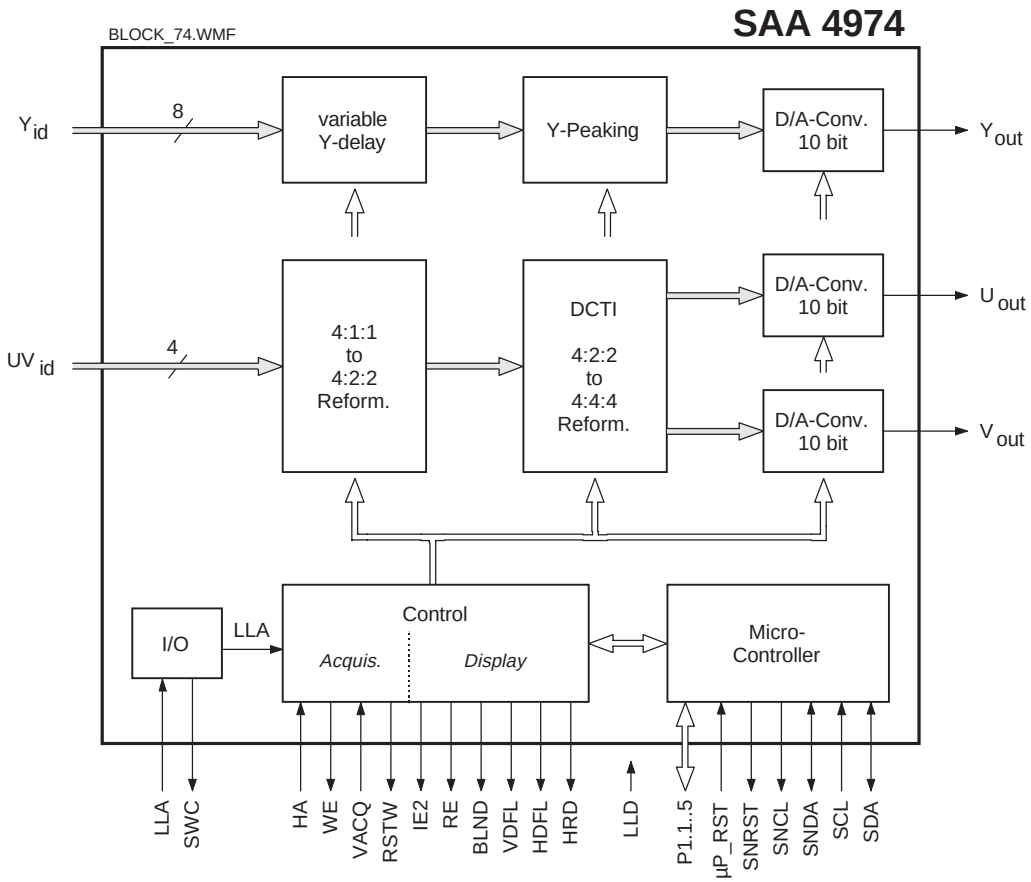


Fig. 18 Block diagram of the SAA 4974

Compared to the SAA 4977 a variable luminance delay is added. This delay permits to compensate any delay differences that may have accumulated so far. The zero delay setting is meant for the nominal case of aligned input data according to the interface format standard. The other settings provide one to seven samples less delay of the luminance signal.

4. see also: Waterholter, Heinrich: The SNERT bus specification, Philips Semiconductors Application Note AN 95127

6. Functional description of the SAA 4991

The MK9 board can be run with the SAA 4977/74 and one field memory, or a second field memory and the SAA 4991 can be added. In this case a lot more functions and features are available. The diagram in fig. 19 gives an overview of the main processing blocks.

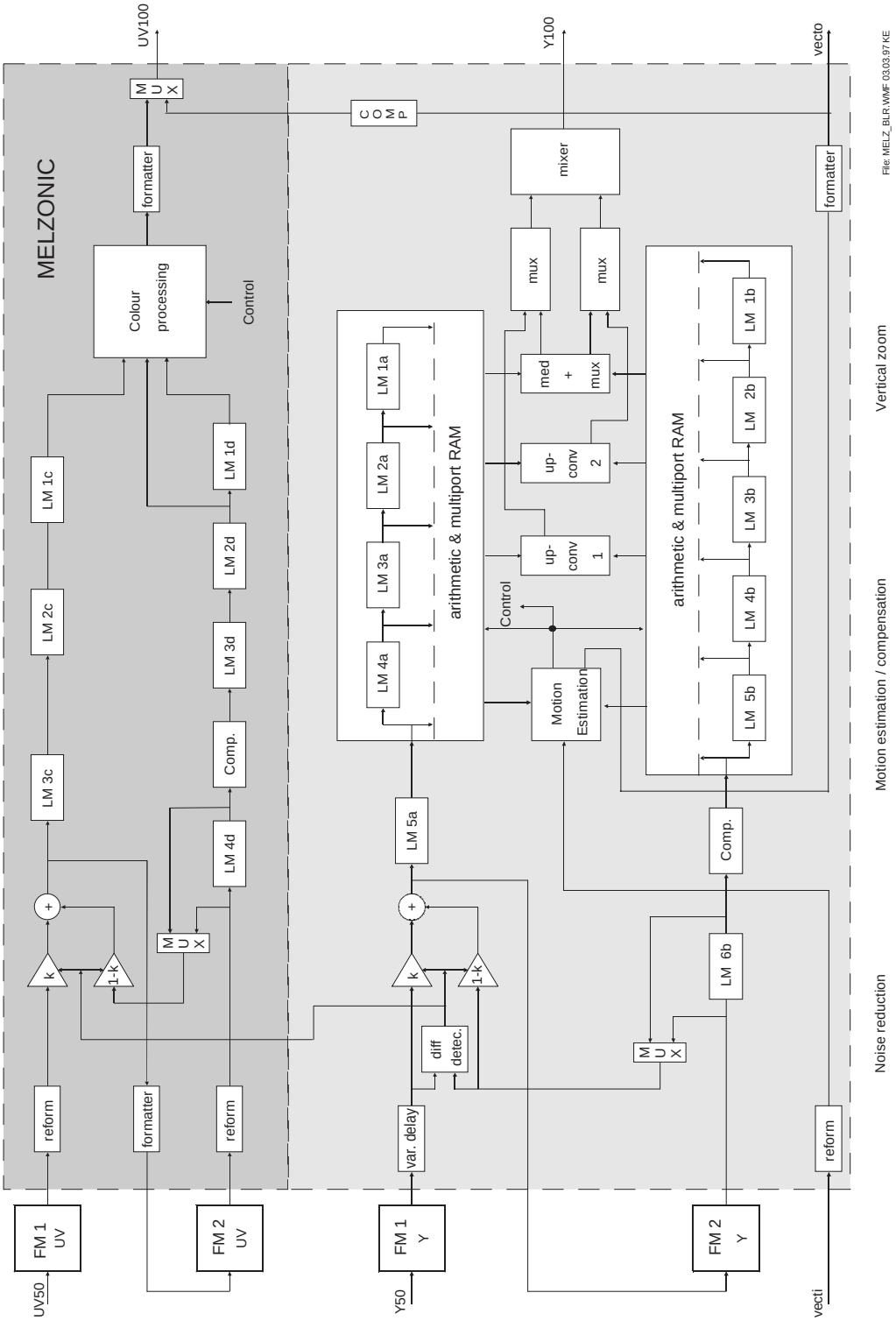


Fig. 19
Block diagram
of the SAA 4991

The SAA 4991 uses two field memories. The first one does the 50Hz/100Hz scan conversion, the second is used for noise reduction, line flicker reduction and motion compensation. Noise reduction is done in the luminance as well as in the chrominance channel. Motion compensation is performed in the luminance signal only, since experiments have shown that the dynamic resolution of chrominance is almost completely masked by luminance. So a chrominance processing based on line-flicker elimination using a three tap median filter is implemented.

6.1 Problems in motion portrayal with picture rate conversion

The main feature of the SAA 4991 is its ability to improve motion portrayal in 100 Hz TVs and to eliminate one of the main artefacts of conventional scan converted images: blurring at moving edges.

The simplest approach to double the scan rate is to display each field twice. This is depicted in fig. 20. For a moving object it can be seen that its position is incorrectly represented in every second field. If the viewer tracks the object it is perceived double, as it´s location in every second field is not at the expected position.

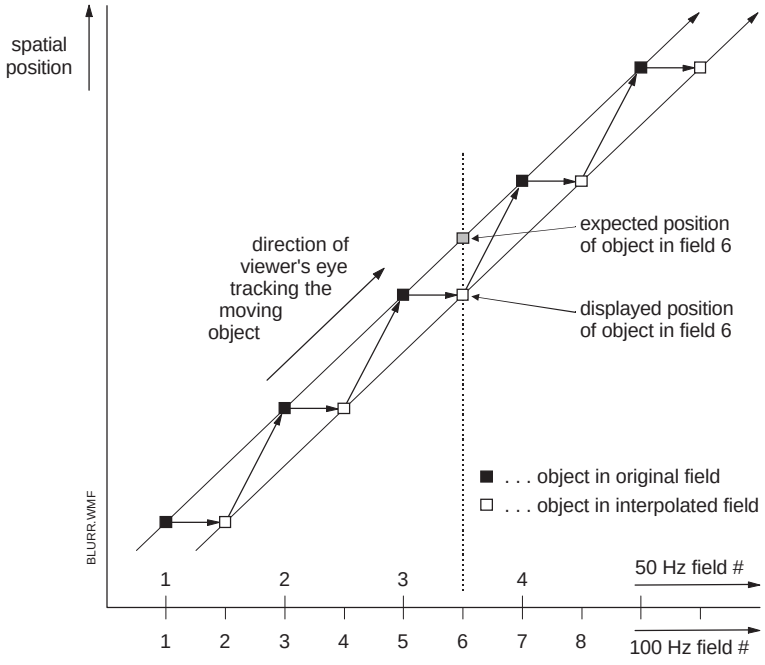


Fig. 20 100 Hz field repetition causes blurring at moving edges

Much worse is the display of movie material on a TV receiver or even in the cinema, because motion comes in a rate of only 25 pictures per second. On a 50 Hz TV each motion phase is displayed twice resulting in annoying jerky motion due to a lower picture update rate and therefore a larger position error between expected and displayed object position. In current 100 Hz TV each movie picture is repeated four times.

6.2 Motion estimation

In order to overcome the above described problems a motion estimation technique is needed, so that objects in the interpolated image can be placed at the position expected by the viewer´s eye. The technique implemented in the SAA 4991 is based on a 3-D recursive search block-matching algorithm.

The picture is divided into blocks of 8 x 8 pixels, and for each block a movement vector is stored in the chip´s vector prediction memory. Calculation of new vectors is mainly based on these previous vectors.

The motion estimator applies two concurrent recursive block matchers that individually check four candidate vectors with different convergence directions. Among the four candidates is one from a previously processed, diago-

nally neighboring block (spatial prediction vector), and one from a block in the previous field (temporal prediction vector). Fig. 21 show this situation. Estimator A checks S_a and T_a, estimator B checks S_b and T_b. The blocks for the temporal prediction vectors are diagonally opposite to the ones for the spatial prediction vectors, and not neighboring but in a larger distance in the same direction. This can improve convergence speed.

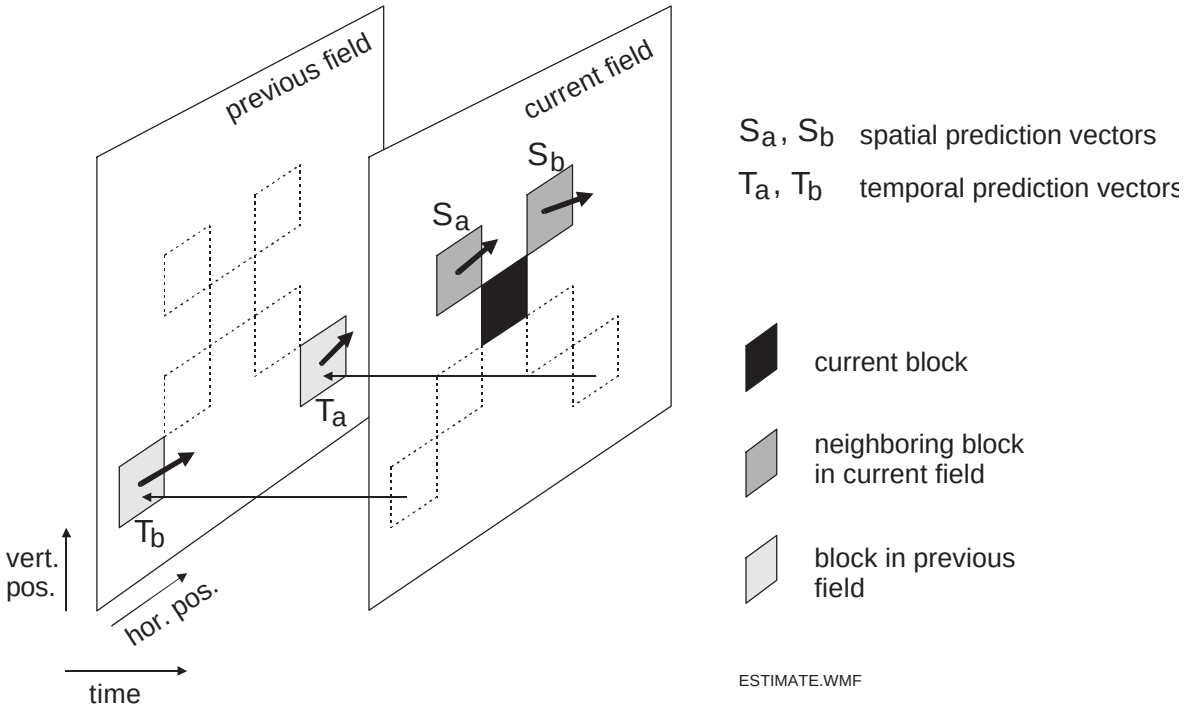


Fig. 21 Position of the spatial and temporal prediction vectors in relation to the currently processed block

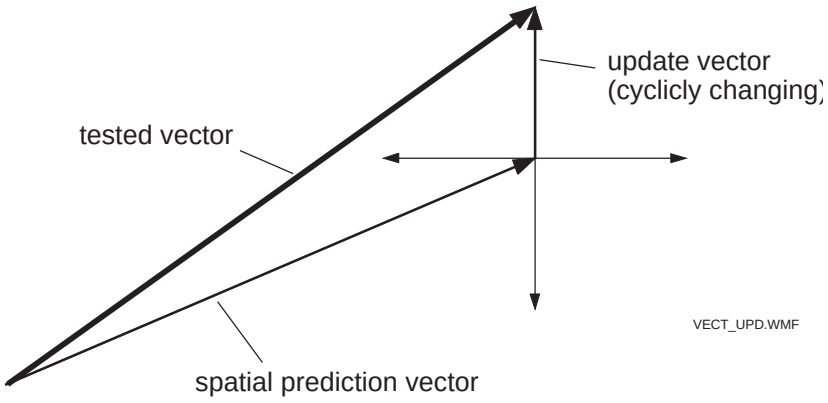


Fig. 22 Recursive search trying to find a better vector

Besides these two vectors each estimator also tests a candidate that is the sum of the spatial prediction vector and an update vector. This update vector is cyclicly chosen from a limited set of vectors with different direction and length. The forth vector tested by each estimator is the vector 0.

Due to limited number of candidates, the recursion of the algorithm and the fact that only a limited update of the prediction value is allowed, the estimation generates a smooth rather than accurate vector field which is desirable for a temporal interpolation of pictures. Run-in problems are solved by applying two estimators with different prediction directions in parallel. A block matching algorithm with this search strategy requires only modest hardware cost due to the limited number of candidate vectors to be evaluated, yet yields a good performance.

The parameters of the motion estimators are summarized below. ´Range´ really indicates the maximum speed an object on the screen can have. The value is based on the 50 Hz field frequency (20 ms), for the actual motion compensated interpolation on the 100 Hz side (10 ms) only half the range is needed. The larger range in horizontal direction reflects the fact that large horizontal displacements occur more frequently than large vertical ones.

Table 4: Key parameters of the motion estimation

Parameter	Value	Unit
Range	±16 hor., ±9 vert.	pixels / 20 ms
Block size	8 hor. x 8 vert.	pixels
Accuracy	±1	pixel / 20 ms
Candidates	8 (2 x 4)	

6.3 Motion compensation

The motion estimation algorithm is combined with an advanced up-conversion algorithm. The picture information of the motion compensated previous and next fields are fed to a three point median filter together with a third non-motion compensated average sample. The principle is illustrated in fig. 23. In case of correct motion vectors

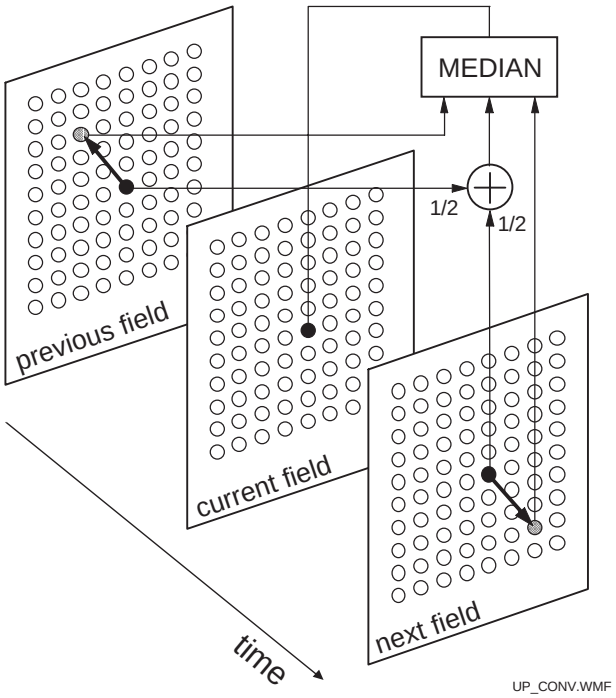


Fig. 23 Implementation of the up-conversion algorithm

the two motion compensated pixels from the neighboring fields are likely to be identical and the median filter will choose one of them. If they differ, which indicates that the motion vectors are unreliable, the chance increases that the non-motion compensated pixel appears at the output. The result is a smooth degradation of picture

material in case of vector failure. On top of this "local fall back" option the chip generates key data on the global reliability of motion vectors. This data is processed by an external microprocessor which, in case of suspect data, can gradually force the upconversion process into a non-motion compensated mode.

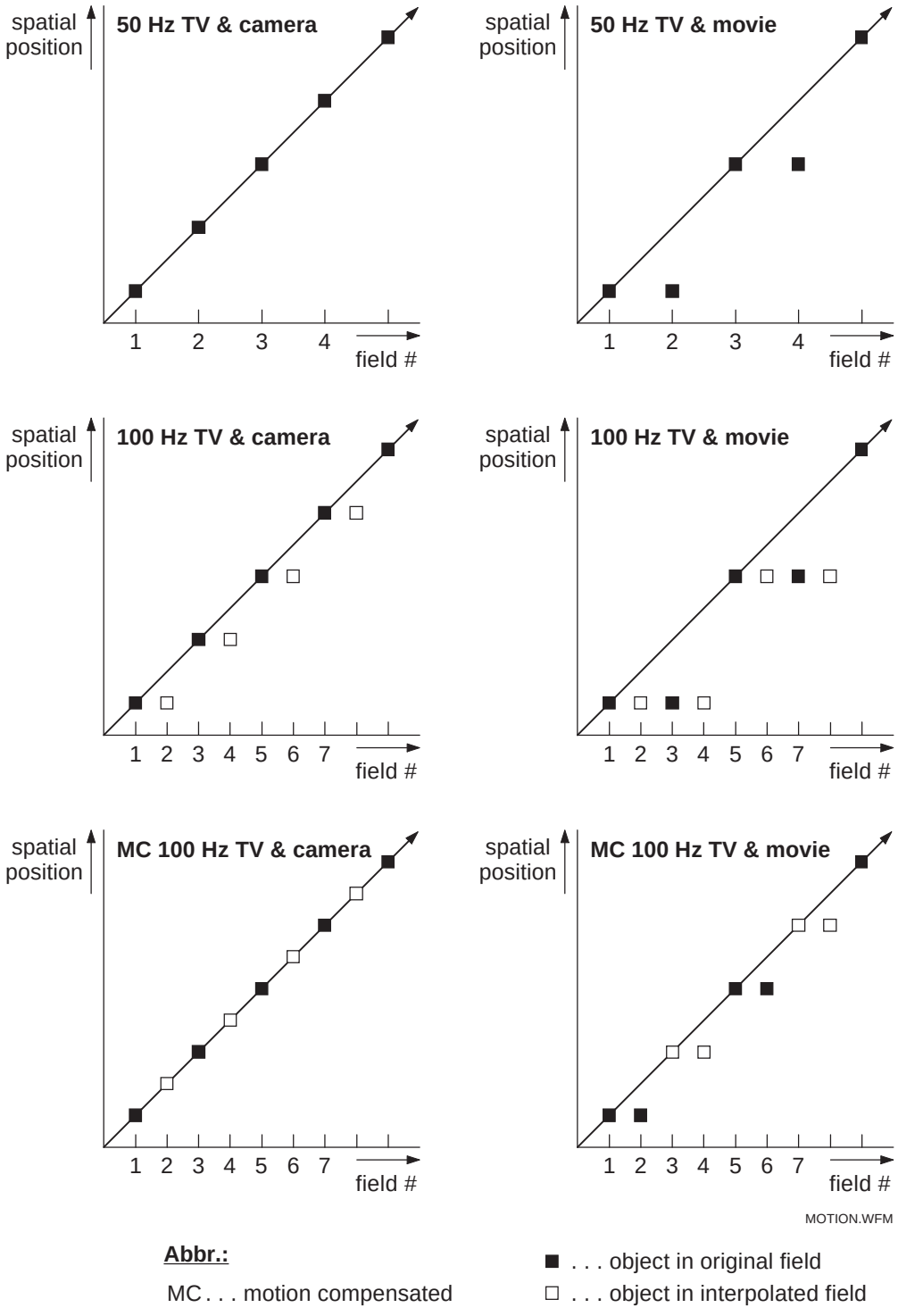


Fig. 24 Portrayal of a moving object on a 50 Hz and 100 Hz TV

Motion estimation and compensation is done not only for up-conversion of video or camera sequences having 50 movements phases per second, but also for converting 25 Hz movie material. In this case both 50 Hz fields are taken from the same movie picture. These 25 movement phases per second are doubled into 50 which is a considerable improvement in movie motion portrayal. Fig. 24 shows the position of a moving object as a function of the output field number for a 50 Hz TV set, a current 100 Hz TV set with field repetition, and a 100 Hz set equipped with the SAA 4991, for both video camera sequences and movie material. As can be seen the SAA 4991 supports a perfect motion compensation for video camera material.

6.4 Motion detection

Because of the different kind of processing for camera and movie mode a discriminator is required to adapt the processing. This discrimination is based on the analysis of motion vectors from the estimator. In movie mode motion will occur only in every second field, so if the sum of absolute vectors is calculated over a field, this sum will vary from field to field in a particular way. The data is fed to an external microcontroller which does the evaluation and determines the mode to be set.

6.5 Vertical Zoom

Vertical zoom is provided by the SAA 4991 in a range between 1.0 and 2.0 in 23 steps. Moreover the zoom factors 3 and 4 are available. An example for a vertical zoom factor of 4/3 = 1.33 in video mode is shown in fig. 25.

For every output field, the up-converter generates odd and even scan lines simultaneously. These lines are either original ones or motion compensated ones from a median filter. Zooming is done by linear interpolation between these odd and even lines, thus for every output field, a progressively scanned frame of 576 active lines (100 Hz) compensated to the correct motion phase, is used. This yields a highly improved performance compared to an intra-field zoom. As shown in fig. 25 the interpolation coefficients repeat in a certain sequence of lines depending on the zoom factor and are also different between fields.

A sequencer is used to control the reading of the field memories, the delay or repetition of the line memory data and the mixing factor of the zoom interpolator. For every output field the microcode for this sequencer is loaded in the chip by the microcontroller. This provides maximum flexibility.

Vertical zoom for chrominance is implemented similarly to luminance. Instead of motion compensated lines line-flicker reduced lines from a median filter are used as input for the interpolator.

6.6 Noise Reduction

Noise reduction is based on a field recursive loop and done for both the luminance and the chrominance signal. The basic scheme is given in fig. 26. New input data and field delayed data are averaged according to the factor K which can range from 0 (still picture) to 1 (noise reduction off). The factor K can be fixed or adaptive. Operation in fixed K mode is possible, but since this can easily lead to smearing along moving edges and fading effects at contrast changes, the adaptive K mode is recommended. In this case the difference in pixel amplitude between the actual and the field delayed input is checked in the luminance channel and taken as the base for selecting a suitable K-factor. Low-pass filtering is performed on these absolute pixel differences, then a user-programmable K-curve (lookup table) is taken to decide on the momentary K-value. A sample K-curve is depicted in fig. 27. It shows that for low pixel differences a low K-value will be taken (strong noise reduction), whereas for pixel differences above 20..30 the K-factor is almost 1 which means that noise reduction is almost turned off.

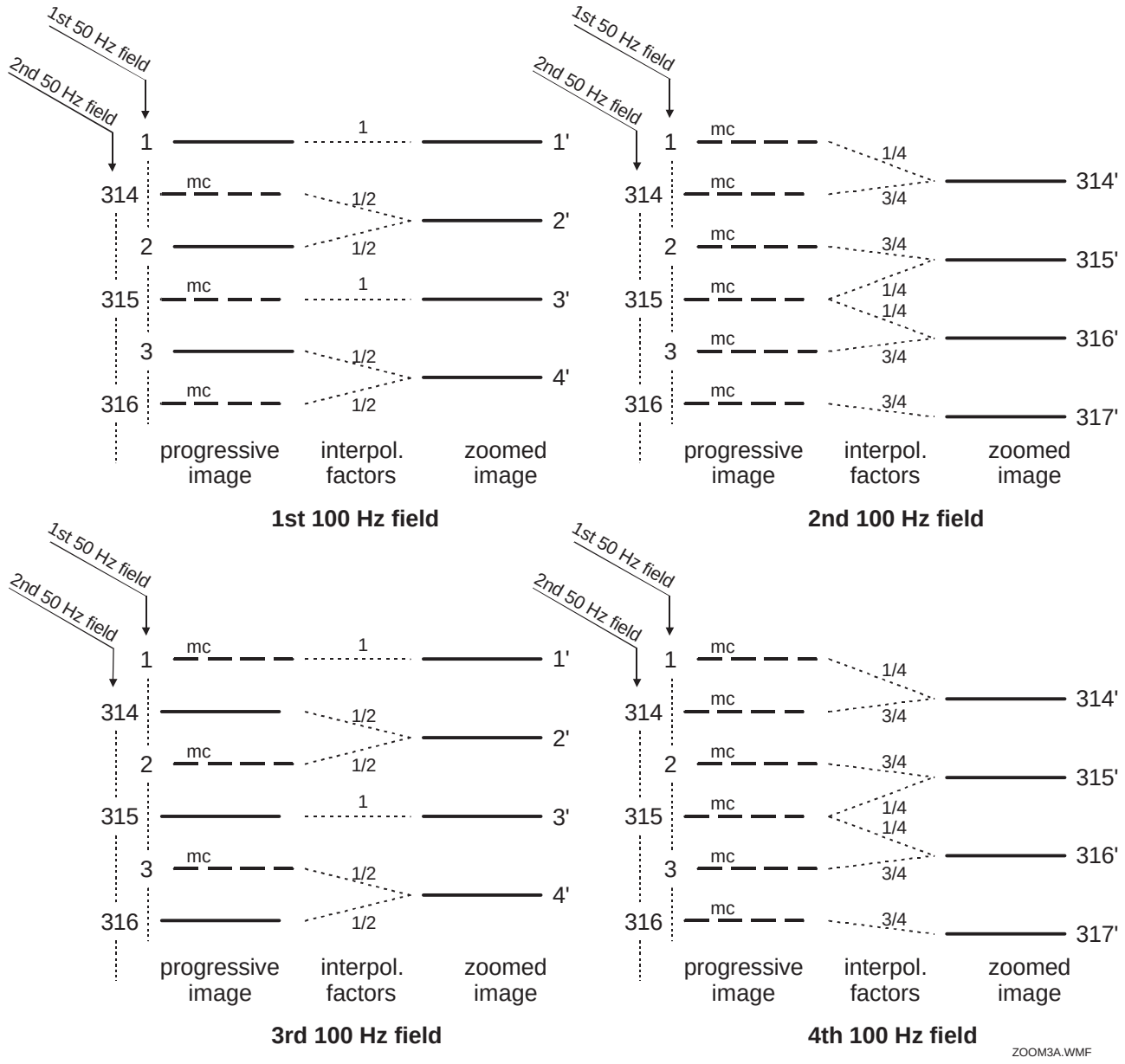


Fig. 25 Zoom sequence of 4/3 in video mode

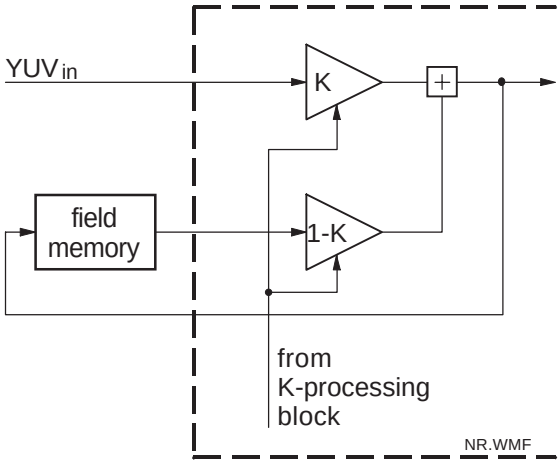


Fig. 26 Noise reduction basic scheme

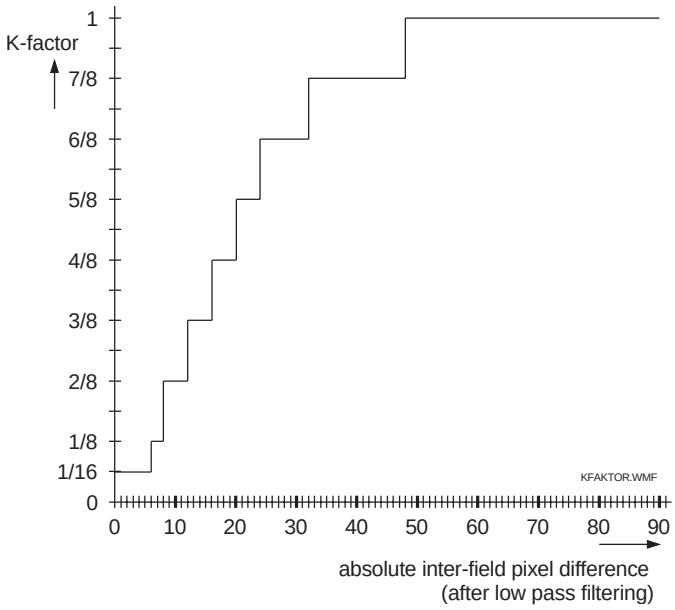


Fig. 27 Example of an adaptive K-curve

7. MK9 Application Board

The SAA 4977 provides the interfaces between the internal digital processing and the analog environment. Luminance and color difference signals from a color decoder or other analog source can be directly input without any external filters. 10 bit D/A converters at the output provide the interface to an RGB processing circuit.

If the board is used with an SAA 4974 no analog input processing is available. In this case the digital data as well as the clock LLA, horizontal sync HA (ABK) and vertical sync can be input through a separate connector.

While the internal functions along the data path are always available, special 100 Hz features depend on external digital components. The simplest form of scan rate conversion is field repetition (A-A-B-B mode), this is possible with just one field memory of the SAA 4955 type connected. A block diagram of this configuration is shown in fig. 28.

An alternative of the SAA 4955 is the compatible SAA 4956. It is the same memory, but with a built-in field-based noise reduction circuit. The noise reduction function can be controlled by I^2C-bus. At the time this report is written the SAA 4956 is still in development.

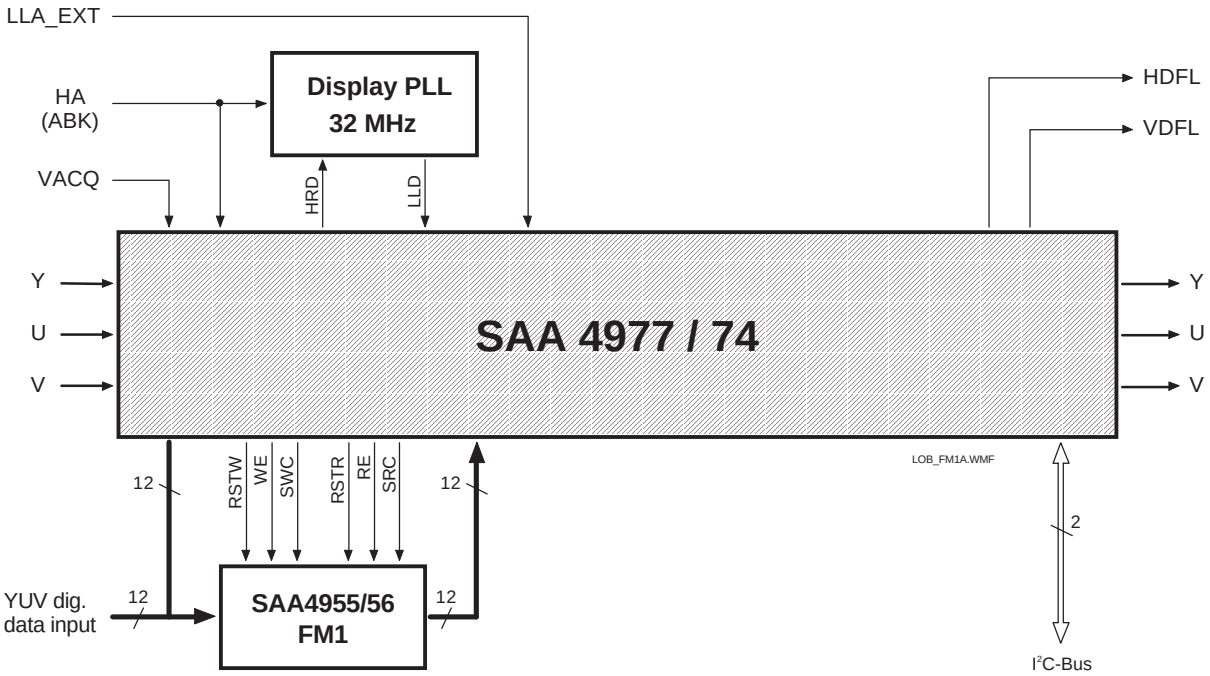


Fig. 28 Application block diagram of the SAA 4977 / 74 using one field memory

Additional functions like motion compensation, line flicker reduction (LFR), progressive scan, zoom and noise reduction are available if the IC SAA 4991 as well as a second field memory SAA 4955 is added. A block diagram of this configuration is shown in fig. 29.

Many functions are realized by software, so for an exact overview of what modes and features are available to the user refer to the appropriate software user manual.

An application board has been prepared to show the functions of the SAA 4977 / SAA 4974. It supports all configurations described above. The complete circuit diagrams are given in fig. 30 to fig. 34. 0-Ohm resistors are used to close the data path in case of the 1-field-memory concept, when no SAA 4991 is present, and also provisions are made on the board to use the SAA 4956 instead of the SAA 4955.

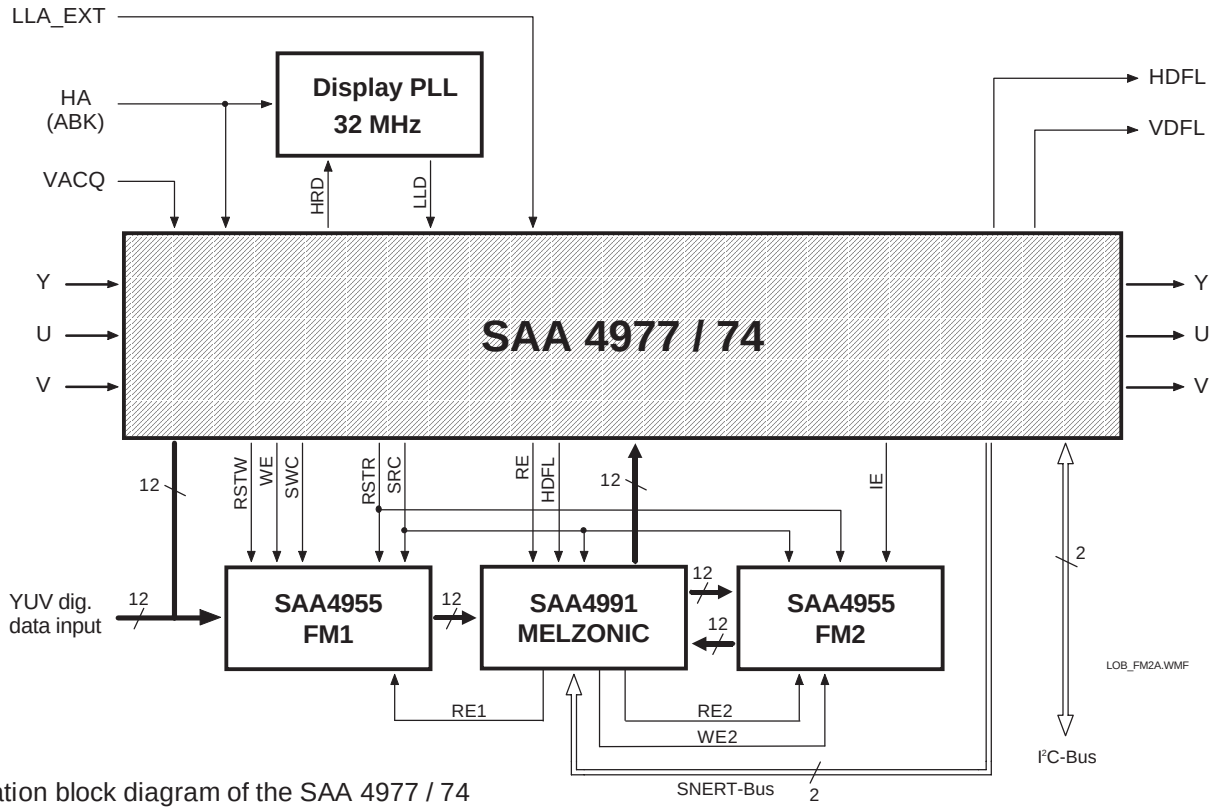


Fig. 29
Application block diagram of the SAA 4977 / 74 using two field memories and the SAA 4991

The SAA 4977 has several power pins for analog and digital supply both at 5V as well 3.3V, see table 5. As can be seen on sheet 5 of the circuit diagram (fig. 34), each positive supply has its own decoupling circuitry. Decoupling capacitors are spread across a large value range, so a wide-band suppression of supply noise is ensured. The positive supply voltages are fed through an inner layer of the 4-layer board, the other inner layer is completely reserved for ground. These two layers are closely on top of each other and thus further improve supply stability.

Table 5: Analog and digital supply pins

Analog supply		Digital supply	
+3.3 VA	**+5 VA**	**+3.3 VD**	**+5 VD**
pin 75: V_{DDA4}	pin 23: V_{DDA1}	pin 8: V_{DDD5}	pin 18: V_{DDD1}
pin 80: V_{DDA5}	pin 25: V_{DDA2}	pin 11: V_{DDD4}	pin 19: V_{DDD0}
	pin 29: V_{DDA3}	pin 69: V_{DDD3}	pin 46: V_{DDD2}
			pin 67: V_{DDIO}

Special care is taken to supply the PLL circuit. Its voltage of +5VP has its own stabilizer. +8VA is used for the analog output amplifiers and filters.

For testing and measurements of the SAA 4977 several power supply lines are equipped with test pins, and provisions are made to break up the on-board supply for external feeding. Input and output signals as well as a few other signals are also provided with test pins for easy monitoring.

The 4-layer board measures 120 mm by 88 mm, the layout of each layer is given in fig. 35 to fig. 38, fig 39 shows the assembly plan of the board.

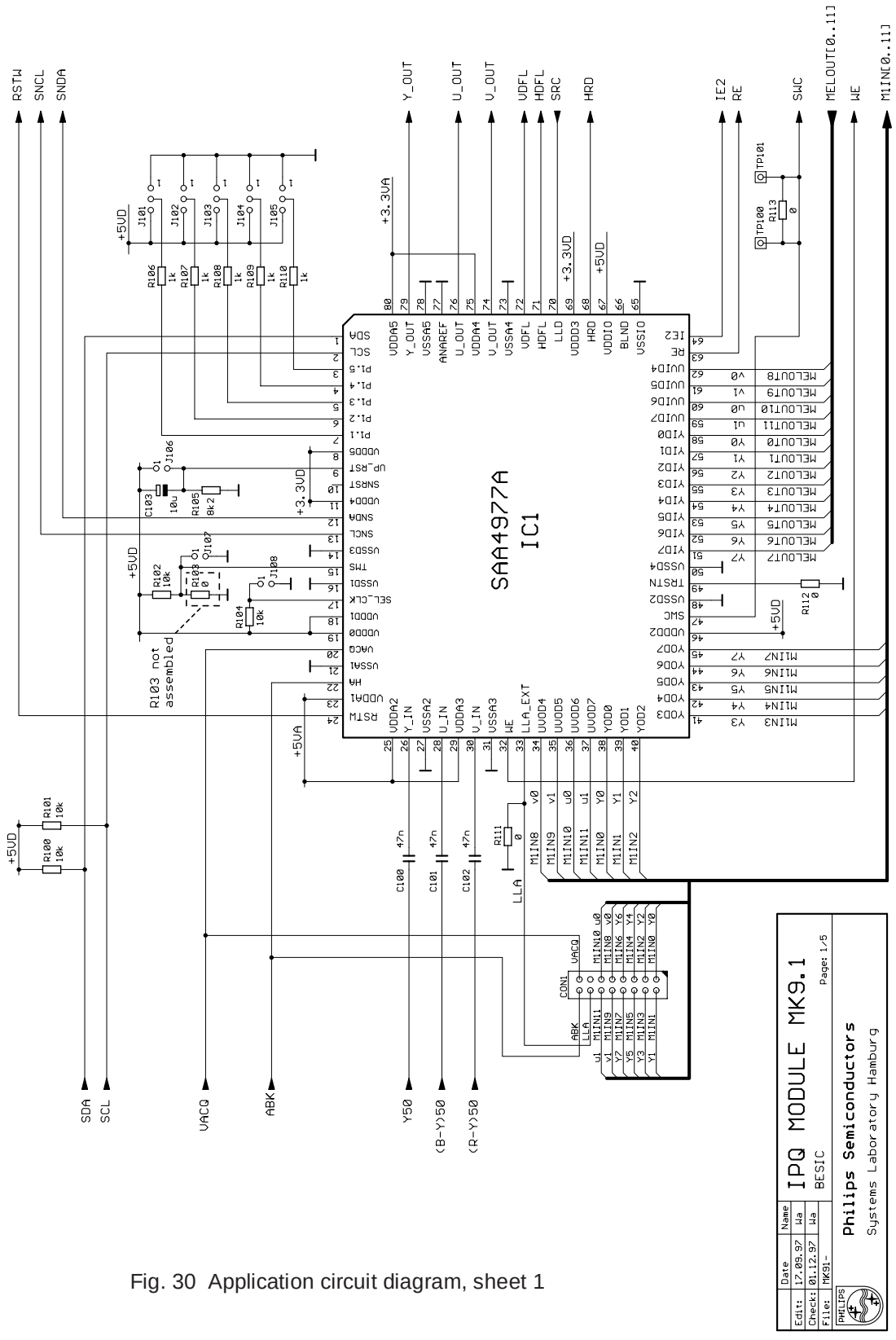


Fig. 30 Application circuit diagram, sheet 1

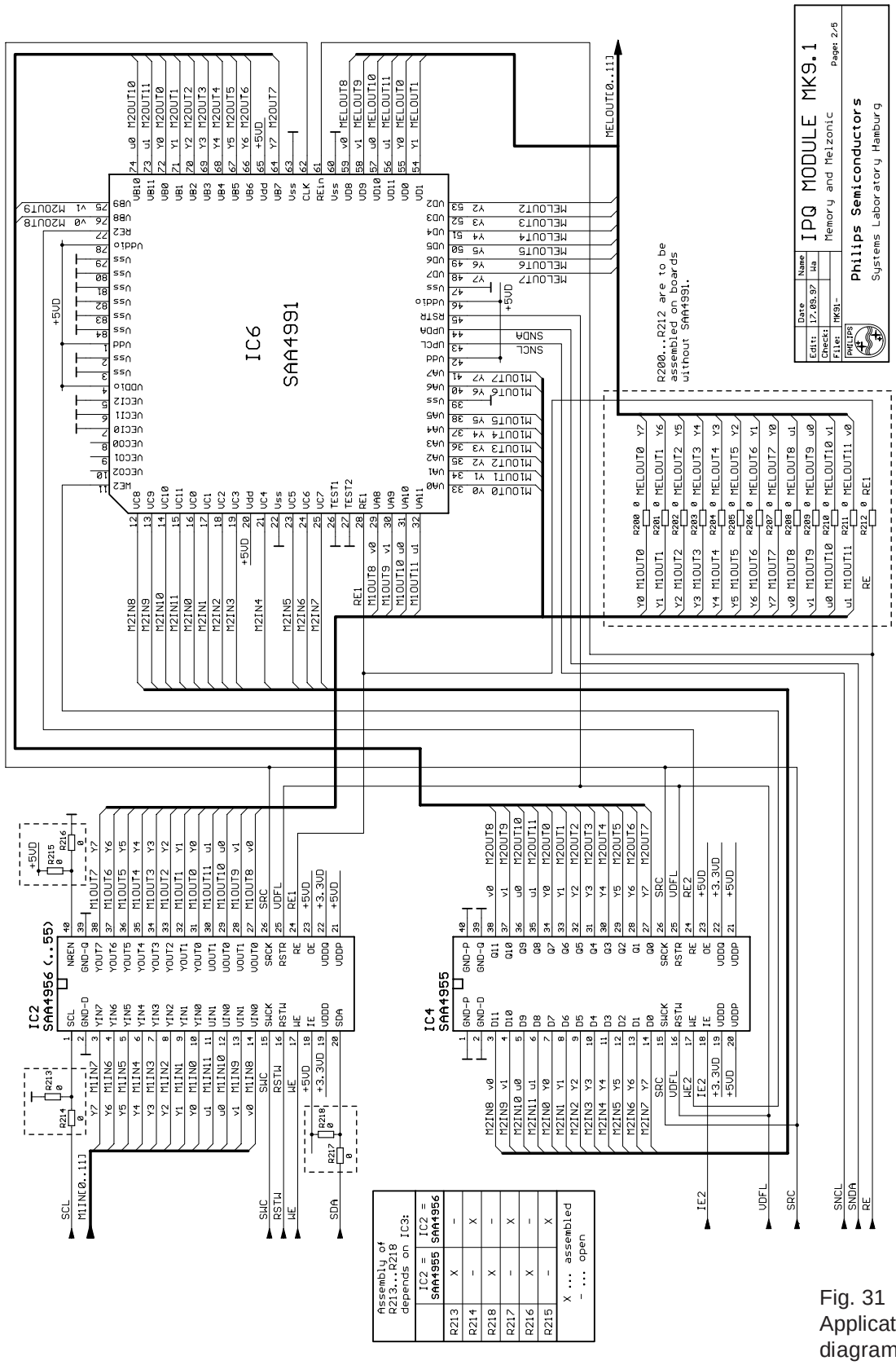


Fig. 31
Application circuit diagram, sheet 2

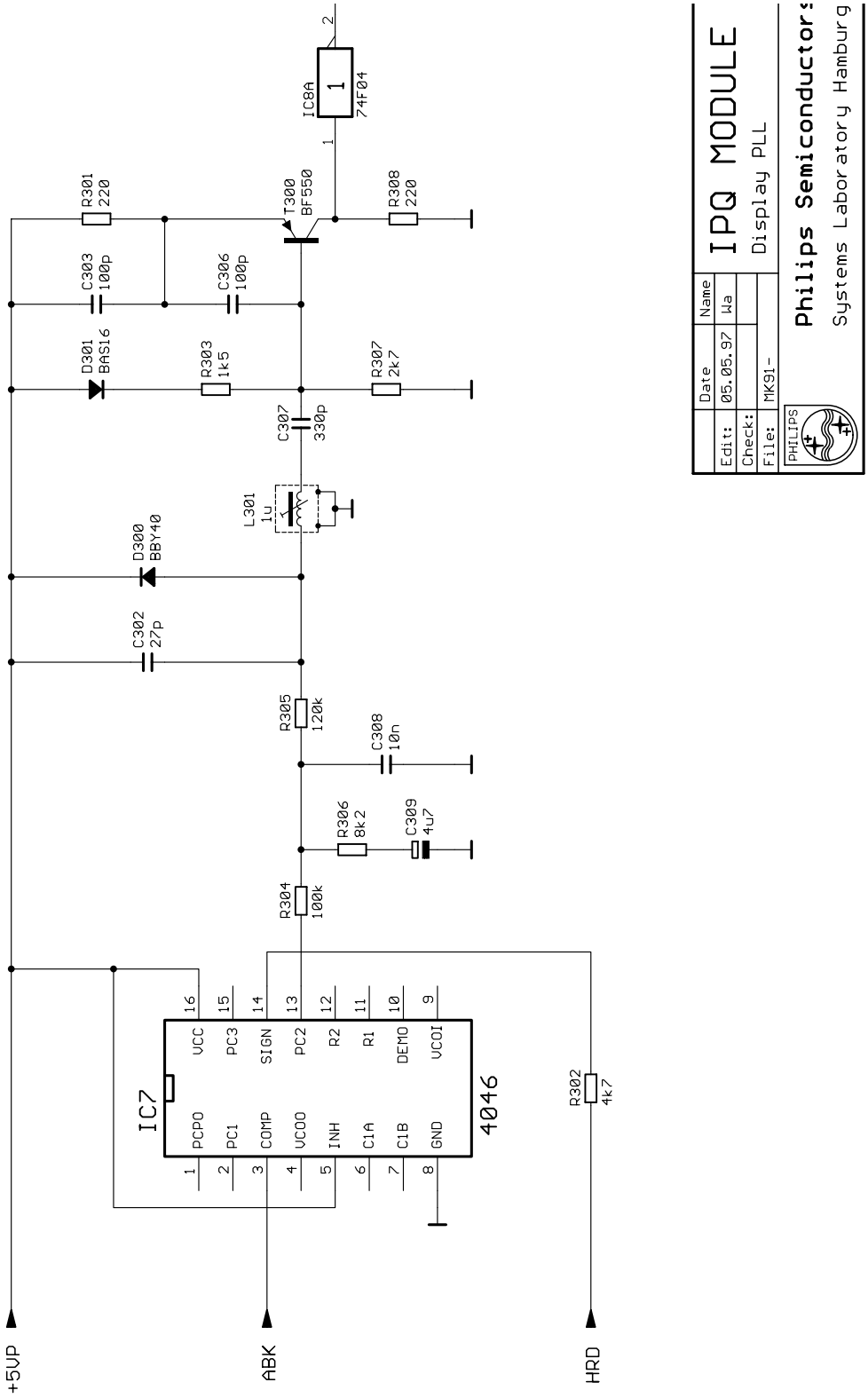


Fig. 32
Application circuit diagram, sheet 3

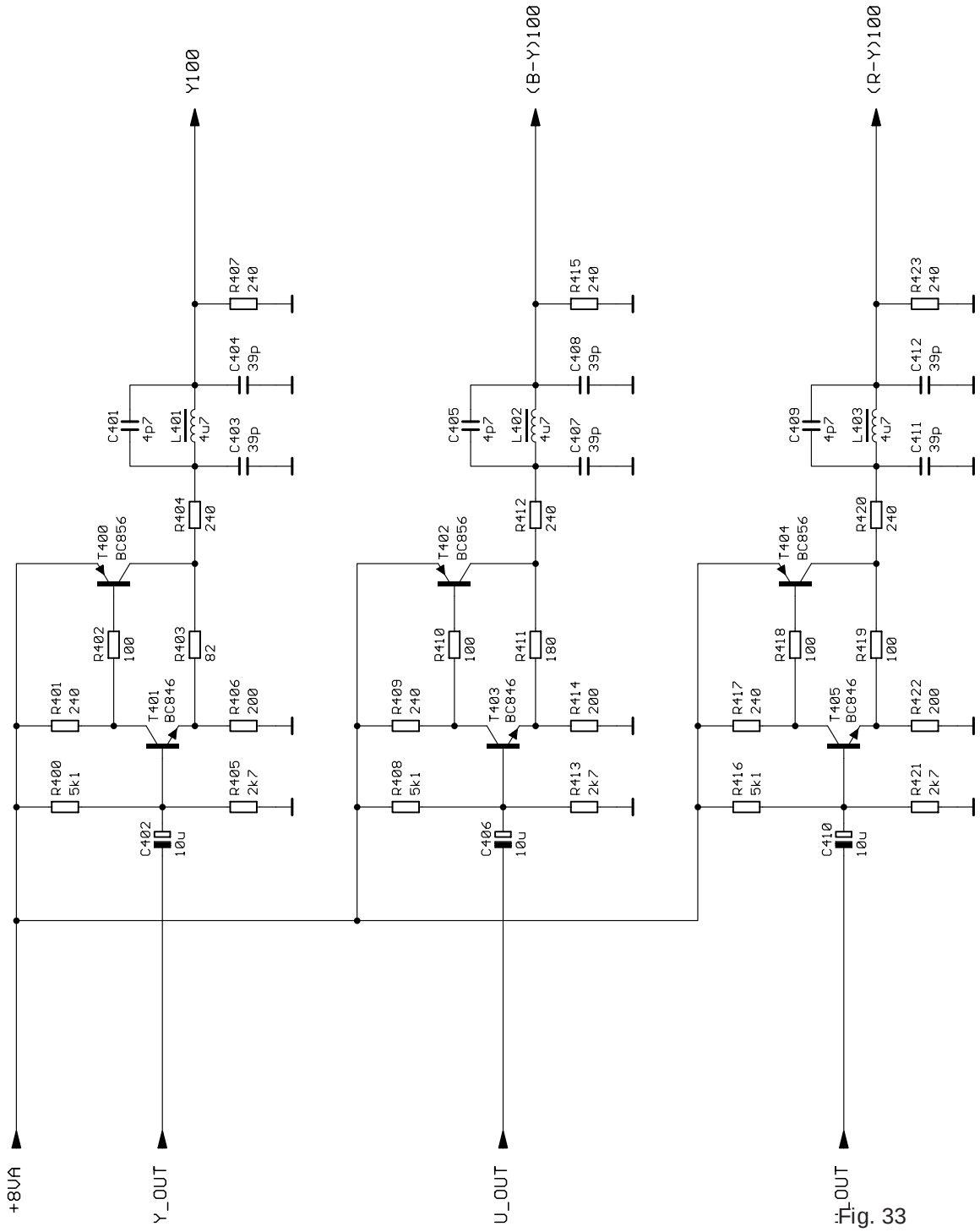


Fig. 33
Application circuit diagram, sheet 4

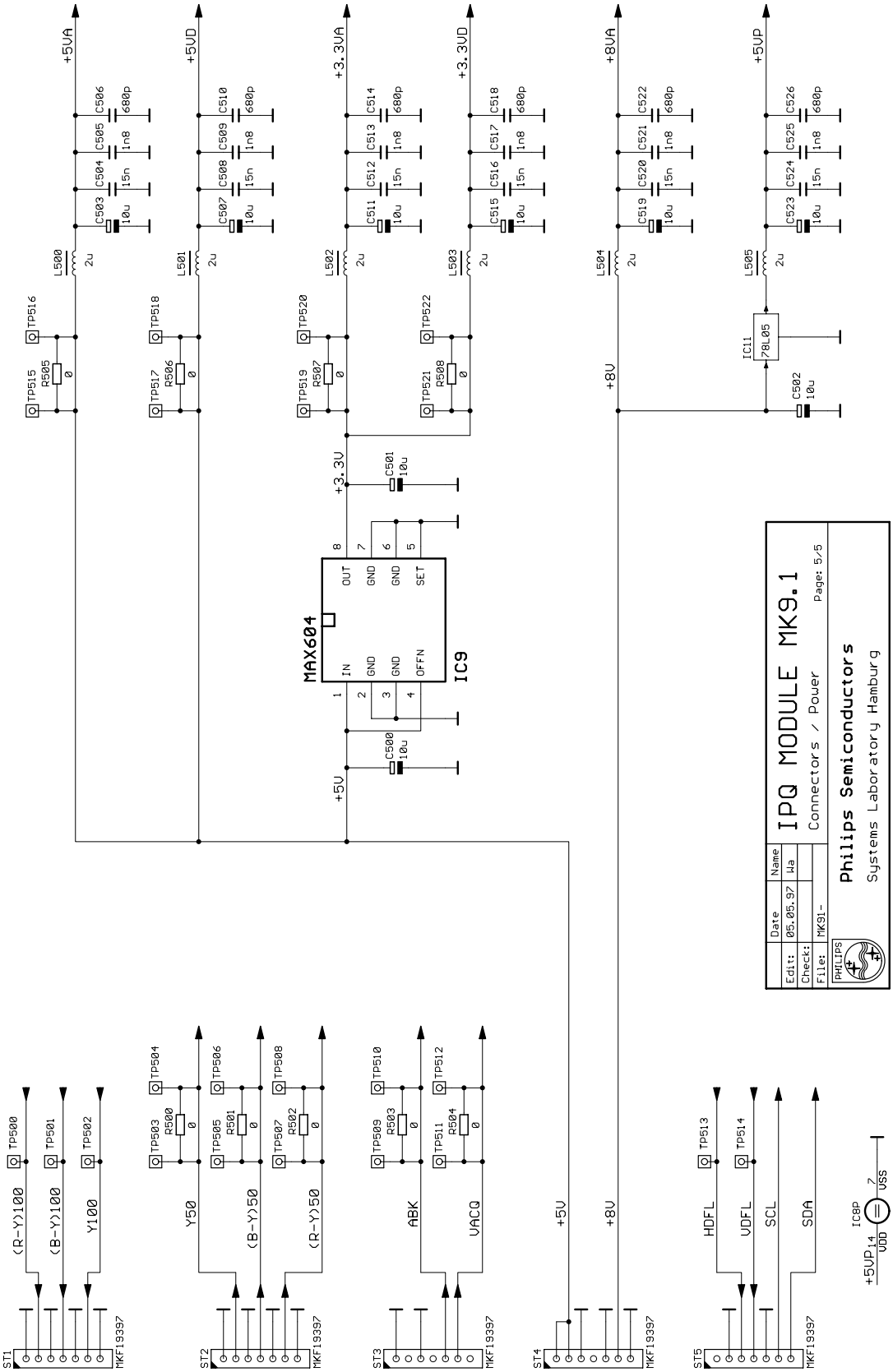


Fig. 34
Application circuit diagram, sheet 5

8. References

[1] Lahann, Nils: I^{2}C-bus register specification for BESIC, Philips Semiconductors User Manual UM9701, 1997

[2] Waterholter, Heinrich: The SNERT bus specification, Philips Semiconductors Application Note AN95127, 1996

[3] The I^{2}C-bus and how to use it, Philips Semiconductors, 1992

[4] SAA 4991 (MELZONIC) data sheet, Philips Semiconductors (preliminary)

[5] True Motion Estimation with 3-D Recursive Search Block-Matching, IEEE Tr. on Circuits & Systems for Video Technology, Vol 3, October 1993

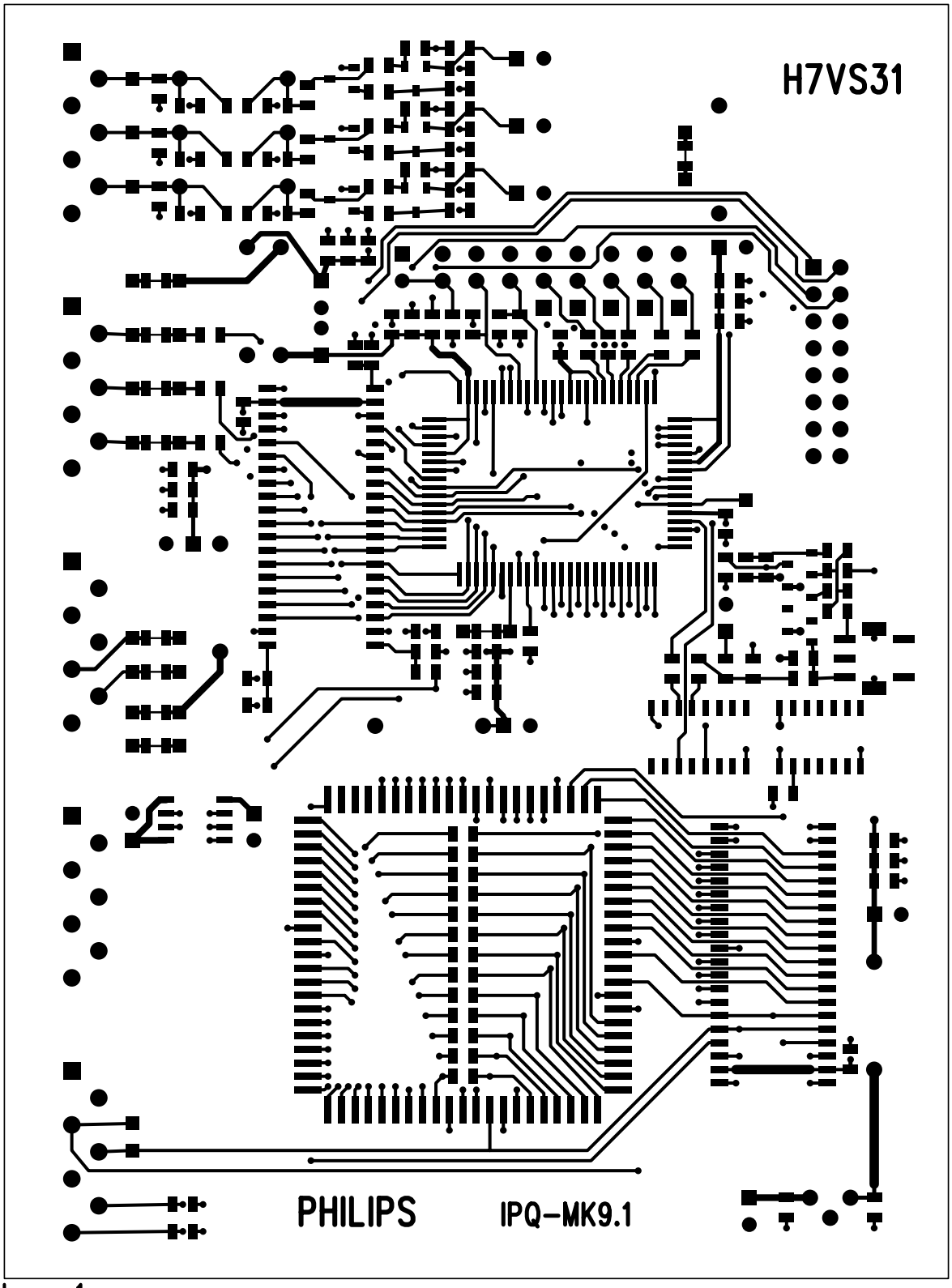


Fig. 35 PC board layout, layer 1 (top)

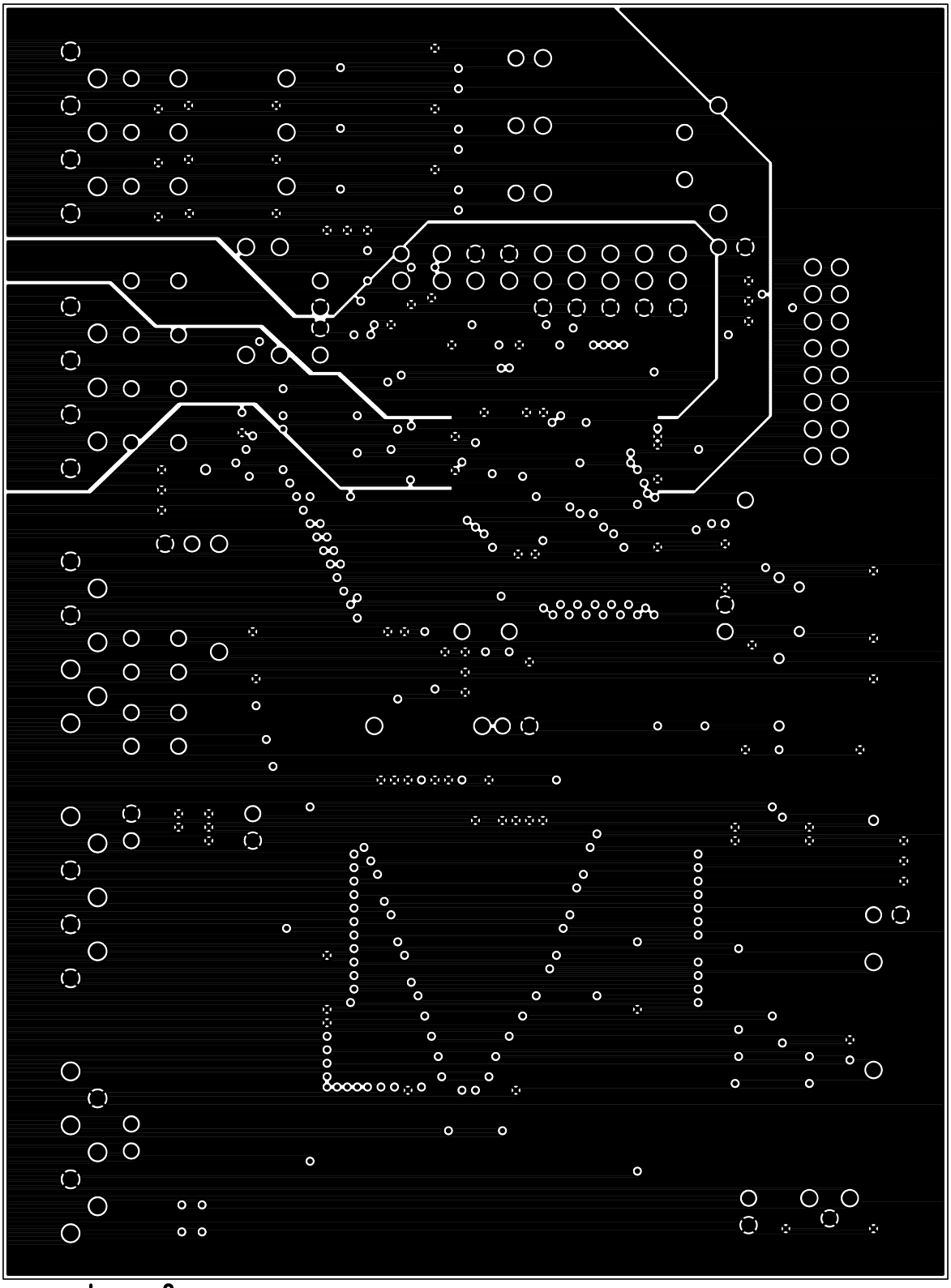


Fig. 36 PC board layout, layer 2

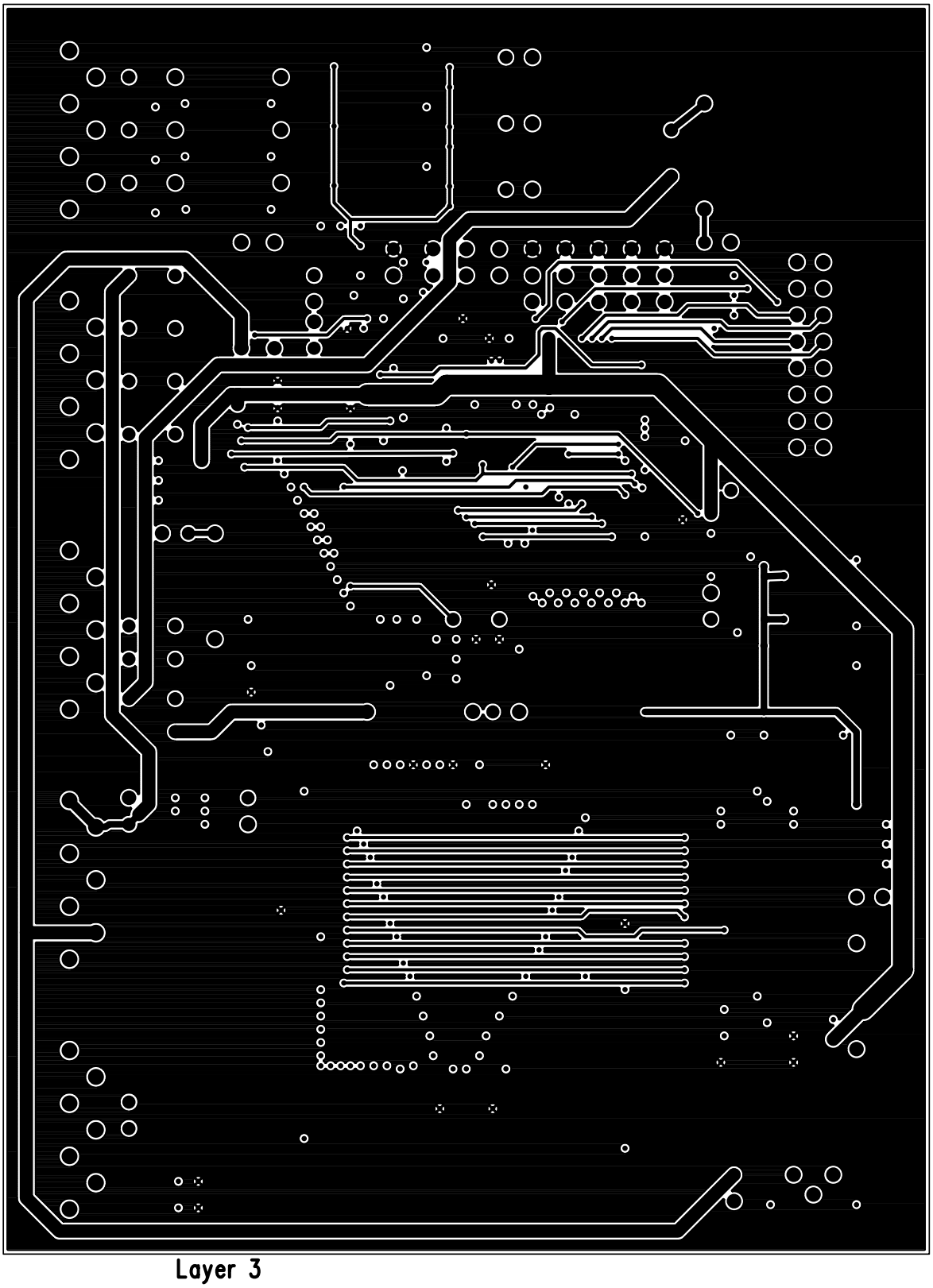


Fig. 37 PC board layout, layer 3

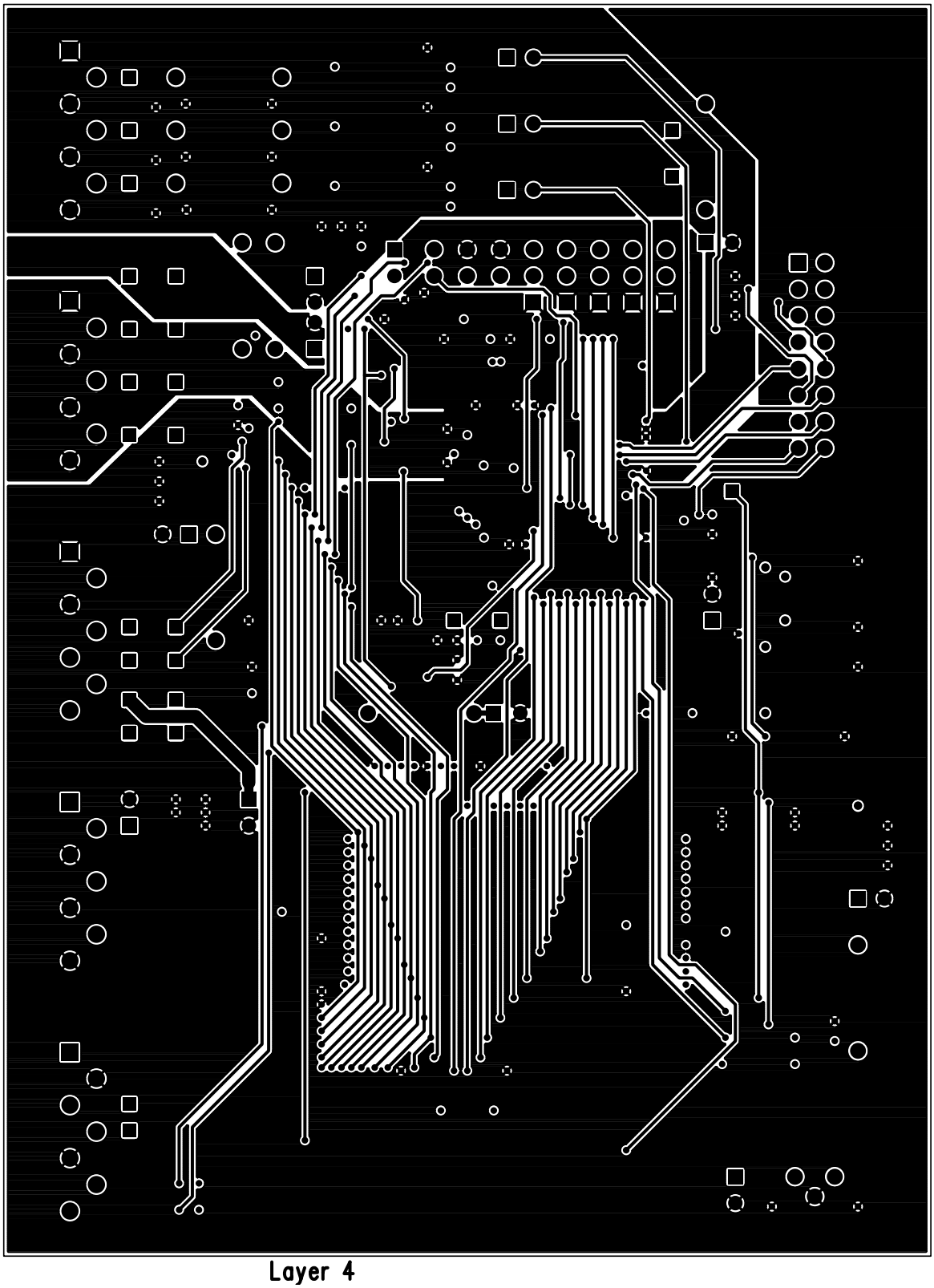


Fig. 38 PC board layout, layer 4 (bottom)

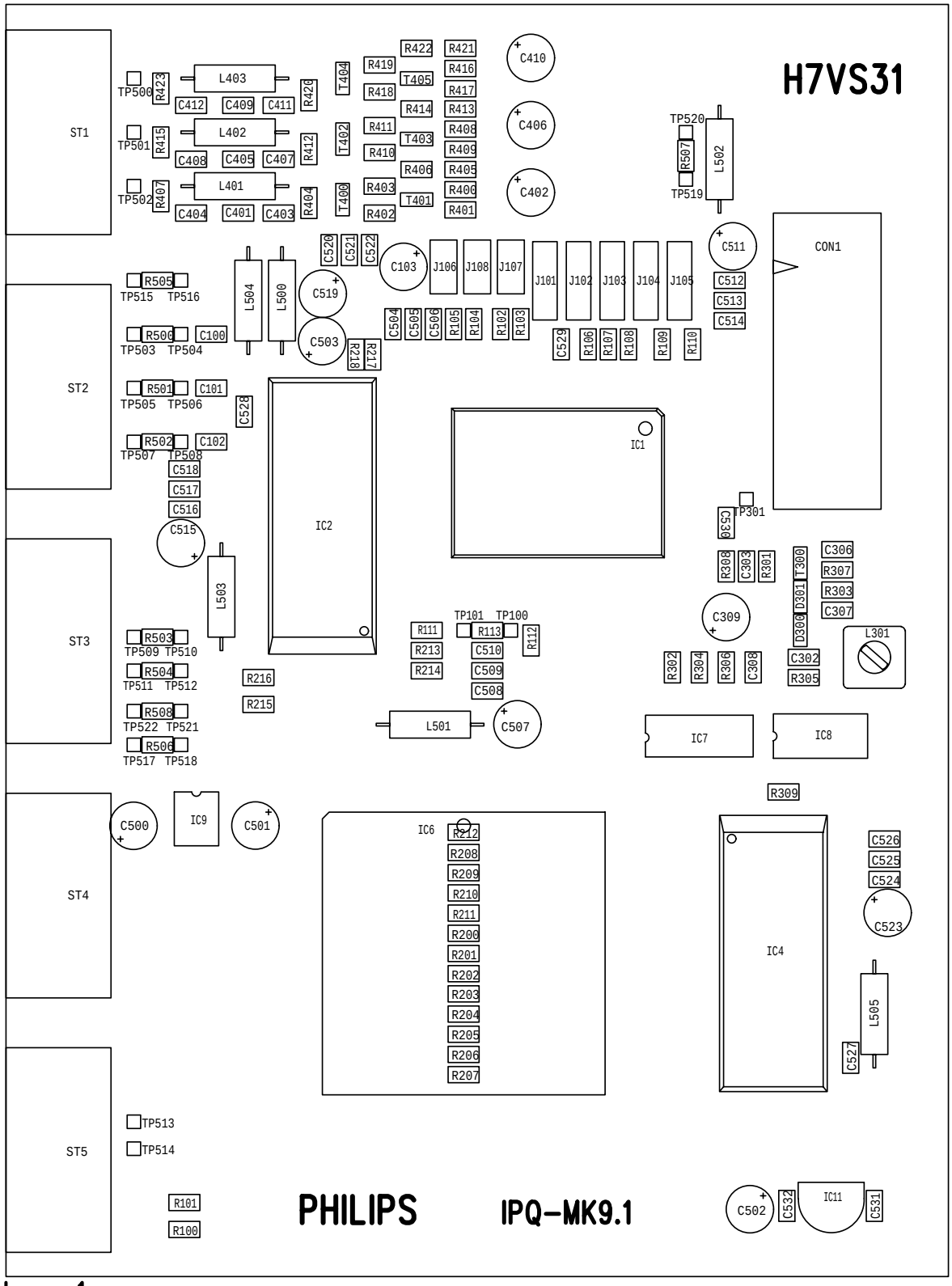


Fig. 39 PC board layout, assembly plan